# SEMESTER 5-6

## Electronics Engineering (VLSI Design and Technology)

| **SEMESTER V ( B Tech VLSI Design and Technology)** | | | | | | |
|---|---|---|---|---|---|---|
| **SLOT** | **COURSE NO.** | **COURSES** | **L-T-P** | **HOURS** | **CREDIT** | **REMARKS** |
| A | ECT 301 | LINEAR INTEGRATED CIRCUITS | 3-1-0 | 4 | 4 | **Same as ECT 301** |
| B | EVT 303 | FPGA BASED SYSTEM DESIGN | 3-1-0 | 4 | 4 | SYLLABUS ATTACHED |
| C | EVT 305 | ***DIGITAL CMOS DESIGN*** | 3-1-0 | 4 | 4 | ,, |
| D | EVT 307 | VLSI TECHNOLOGY | 3-1-0 | 4 | 4 | ,, |
| E<br>1/2 | HUT300 | INDUSTRIAL ECONOMICS AND<br>FOREIGN TRADE | 3-0-0 | 3 | 3 | **EXISTING SYLLABUS** |
| | HUT310 | MANAGEMENT FOR ENGINEERS | 3-0-0 | 3 | 3 | ,, |
| F | MCN301 | DISASTER MANAGEMENT | 2-0-0 | 2 | -- | ,, |
| S | ECL331 | ANALOG INTEGRATION CIRCUITS AND SIMULATION LAB | 0-0-3 | 3 | 2 | Same as ECL 331 |
| T | EVL 333 | RECONFIGURABLE COMPUTING LAB | 0-0-3 | 3 | 2 | SYLLABUS ATTACHED |
| R/M/H | VAC | Remedial/Minor/Honours course | 3-1-0 | 4** | 4 | |
| TOTAL | | | | **27/31** | **23/27** | |

| ECT301 | LINEAR INTEGRATED CIRCUITS | CATEGORY | L | T | P | CREDITS |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:** This course aims to develop the skill to design circuits using operational amplifiers and other linear ICs for various applications.

**Prerequisite**: EC202 Analog Circuits

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO 1** | Understand Op Amp fundamentals and differential amplifier configurations |
| **CO 2** | Design operational amplifier circuits for various applications |
| **CO 3** | Design Oscillators and active filters using opamps |
| **CO4** | Explain the working and applications of timer, VCO and PLL ICs |
| **CO5** | Outline the working of Voltage regulator IC's and Data converters |

**Mapping of course outcomes with program outcomes**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO 1** | 3 | 3 | 1 | 2 | | | | | | | | 1 |
| **CO 2** | 3 | 3 | 2 | 2 | 2 | | | | | | | 1 |
| **CO 3** | 3 | 3 | 2 | 2 | 2 | | | | | | | 1 |
| **CO 4** | 3 | 3 | 1 | 2 | 2 | | | | | | | 1 |
| **CO 5** | 3 | 3 | 2 | 2 | 2 | | | | | | | 1 |

**Assessment Pattern**

| Bloom's Category | | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|---|
| | | 1 | 2 | |
| Remember | K1 | 10 | 10 | 10 |
| Understand | K2 | 30 | 30 | 60 |
| Apply | K3 | 10 | 10 | 30 |
| Analyse | K4 | | | |
| Evaluate | | | | |
| Create | | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| **150** | **50** | **100** | **3 hours** |

**Continuous Internal Evaluation Pattern:**

| | |
|---|---|
| Attendance | : 10 marks |
| Continuous Assessment Test (2 numbers) | : 25 marks |
| Assignment/Quiz/Course project | : 15 marks |

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1): Analyze differential amplifier configurations.**

1. Explain the working of BJT differential amplifiers.
2. Calculate the input resistance, output resistance, voltage gain and CMRR of differential amplifiers.
3. Explain the non-ideal parameters of differential amplifiers.
4. Derive CMRR, input resistance and output resistance of a dual input balanced output differential amplifier configuration.

**Course Outcome 2 (CO2): Design operational amplifier circuits for various applications.**

1. Design an opamp circuit to obtain an output voltage $V_0=-(2V_1+4V_2 + 3V_3)$
2. A 741C op-amp is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve of 741C is flat upto 20kHz.What maximum peak to peak input signal can be applied without distorting the output?
3. With the help of a neat circuit diagram, derive the equation for the output voltage of an Instrumentation amplifier.
4. With the help of circuit diagrams and graphs, explain the working of a Full wave Precision rectifier.

**Course Outcome 3 (CO3): Design active filters using opamps**

1. Derive the design equations for a second order Butterworth active low pass filter.
2. Design a Notch filter to eliminate power supply hum (50 Hz).
3. Design a first order low pass filter at a cut-off frequency of 2kHz with a pass band gain of 3

**Course Outcome 4 (CO4): Explain the working and applications of specialized ICs**

1. With the help of internal diagram explain the monostable operation of timer IC 555. Draw the input and different output waveforms. Derive the equation for pulse width.
2. Explain the operation of Phase Locked Loop. What is lock range and capture range? Realize a summing amplifier to obtain a given output voltage.

3. Design a circuit to multiply the incoming frequency by a factor of 5 using 565 PLL.

**Course Outcome 5 (CO5): Outline the working of Voltage regulator IC's and Data converters**

1. What is the principle of operation of Dual slope ADC. Deduce the relationship between analogue input and digital output of the ADC.
2. Explain how current boosting is achieved using I.C 723
3. Explain the working of successive approximation ADC

## SYLLABUS

**Module 1:**

**Operational amplifiers(Op Amps):** The 741 Op Amp, Block diagram, Ideal op-amp parameters, typical parameter values for 741, Equivalent circuit, Open loop configurations, Voltage transfer curve, Frequency response curve.

**Differential Amplifiers:** Differential amplifier configurations using BJT, DC Analysis- transfer characteristics; AC analysis- differential and common mode gains, CMRR, input and output resistance, Voltage gain. Constant current bias, constant current source; Concept of current mirror-the two transistor current mirror, Wilson and Widlar current mirrors.

**Module 2:**

**Op-amp with negative feedback**: General concept of Voltage Series, Voltage Shunt, current series and current shunt negative feedback, Op Amp circuits with voltage series and voltage shunt feedback, Virtual ground Concept; analysis of practical inverting and non-inverting amplifiers for closed loop gain, Input Resistance and Output Resistance.
**Op-amp applications:** Summer, Voltage Follower-loading effects, Differential and Instrumentation Amplifiers, Voltage to current and Current to voltage converters, Integrator, Differentiator, Precision rectifiers, Comparators, Schmitt Triggers, Log and antilogamplifiers.

**Module 3:**

**Op-amp Oscillators and Multivibrators:** Phase Shift and Wien-bridge Oscillators, Triangular and Sawtooth waveform generators, Astable and monostable multivibrators.
**Active filters**: Comparison with passive filters, First and second order low pass, High pass, Band pass and band reject active filters, state variable filters.

**Module 4 :**

**Timer and VCO:** Timer IC 555- Functional diagram, Astable and monostable operations;. Basic concepts of Voltage Controlled Oscillator and application of VCO IC LM566,
**Phase Locked Loop –** Operation, Closed loop analysis, Lock and capture range, Basic building blocks, PLL IC 565, Applications of PLL.

**Module 5:**

**Voltage Regulators:** Fixed and Adjustable voltage regulators, IC 723 – Low voltage and high voltage configurations, Current boosting, Current limiting, Short circuit and Fold-back protection.
**Data Converters:** Digital to Analog converters, Specifications, Weighted resistor type and R-2R Ladder type.
Analog to Digital Converters: Specifications, Flash type and Successive approximation type.

**Text Books**

1. Roy D. C. and S. B. Jain, Linear Integrated Circuits, New Age International, 3/e, 2010

**Reference Books**

1. DFranco S., Design with Operational Amplifiers and Analog Integrated Circuits, 3/e, Tata McGraw Hill, 2008
2. Gayakwad R. A., Op-Amps and Linear Integrated Circuits, Prentice Hall, 4/e, 2010
3. Salivahanan S. and V. S. K. Bhaaskaran, Linear Integrated Circuits, Tata McGraw Hill, 2008.
4. Botkar K. R., Integrated Circuits, 10/e, Khanna Publishers, 2010
5. C.G. Clayton, Operational Amplifiers, Butterworth & Company Publ. Ltd. Elsevier, 1971
6. David A. Bell, Operational Amplifiers & Linear ICs, Oxford University Press, 2nd edition,2010
7. R.F. Coughlin & Fredrick Driscoll, Operational Amplifiers & Linear Integrated Circuits,6th Edition, PHI,2001
8. Sedra A. S. and K. C. Smith, Microelectronic Circuits, 6/e, Oxford University Press, 2013.

**Course Contents and Lecture Schedule**

| No | Topic | No. of Lectures |
|---|---|---|
| **1** | **Operational amplifiers** | **(9)** |
| 1.1 | The 741 Op Amp, Block diagram, Ideal op-amp parameters, typical parameter values for 741 | 1 |
| 1.2 | Equivalent circuit, Open loop configurations, Voltage transfer curve, Frequency response curve. | 1 |
| 1.3 | Differential amplifier configurations using BJT, DC Analysis- transfer characteristics | 2 |
| 1.4 | AC analysis- differential and common mode gains, CMRR, input and output resistance, Voltage gain | 2 |
| 1.5 | Constant current bias and constant current source | 1 |
| 1.6 | Concept of current mirror, the two transistor current mirror Wilson and Widlar current mirrors. | 2 |
| 2 | **Op-amp with negative feedback and Op-amp applications** | **(11)** |

| | | |
|---|---|---|
| 2.1 | General concept of Voltage Series, Voltage Shunt, current series and current shunt negative feedback | 1 |
| 2.2 | Op Amp circuits with voltage series and voltage shunt feedback, Virtual ground Concept | 1 |
| 2.3 | Analysis of practical inverting and non-inverting amplifier | 2 |
| 2.4 | Summer, Voltage Follower-loading effect | 1 |
| 2.5 | Differential and Instrumentation Amplifiers | 1 |
| 2.6 | Voltage to current and Current to voltage converters | 1 |
| 2.7 | Integrator, Differentiator | 1 |
| 2.8 | Precision rectifiers-half wave and full wave | 1 |
| 2.9 | Comparators, Schmitt Triggers | 1 |
| 2.10 | Log and antilog amplifier | 1 |
| **3** | **Op-amp Oscillators and Multivibrators** | **(10)** |
| 3.1 | Phase Shift and Wien-bridge Oscillators, | 2 |
| 3.2 | Triangular and Sawtooth waveform generators, Astable and monostable multivibrators | 2 |
| 3.3 | Comparison, design of First and second order low pass and High pass active filters | 2 |
| 3.4 | Design of Second Order Band pass and band reject filters | 2 |
| 3.5 | State variable filters | 2 |
| **4** | **Timer, VCO and PLL** | **(9)** |
| 4.1 | Timer IC 555- Functional diagram, Astable and monostable operations. | 2 |
| 4.2 | Basic concepts of Voltage Controlled Oscillator | 1 |
| 4.3 | Application of VCO IC LM566 | 2 |
| 4.4 | PLL Operation, Closed loop analysis Lock and capture range. | 2 |
| 4.5 | Basic building blocks, PLL IC 565, Applications of PLL | 2 |
| **5** | **Voltage regulators and Data converters** | **(9)** |
| 5.1 | Fixed and Adjustable voltage regulators | 1 |
| 5.2 | IC 723 – Low voltage and high voltage configurations, | 2 |
| 5.3 | Current boosting, Current limiting, Short circuit and Fold-back protection. | 2 |
| 5.4 | Digital to Analog converters, Specifications, Weighted resistor type and R-2R Ladder type. | 2 |
| 5.5 | Analog to Digital Converters: Specifications, Flash type and Successive approximation type. | 2 |

**Assignment:**

Assignment may be given on related innovative topics on linear IC, like Analog multiplier- Gilbert multiplier cell, variable trans-conductance technique, application of analog multiplier IC AD633., sigma delta or other types of ADC etc. At least one assignment should be simulation of opamp circuits on any circuit simulation software. The following simulations can be done in QUCS, KiCad or PSPICE.(The course instructor is free to add or modify the list)

1. Design and simulate a BJT differential amplifier. Observe the input and output signals. Plot the AC frequency response
2. Design and simulate Wien bridge oscillator for a frequency of 10 kHz. Run a transient simulation and observe the output waveform.
3. Design and implement differential amplifier and measure its CMRR. Plot its transfer characteristics.
4. Design and simulate non-inverting amplifier for gain 5. Observe the input and output signals. Run the ac simulation and observe the frequency response and 3− db bandwidth.
5. Design and simulate a 3 bit flash type ADC. Observe the output bit patterns and transfer characteristics
6. Design and simulate R − 2R DAC circuit.
7. Design and implement Schmitt trigger circuit for upper triggering point of +8 V and a lower triggering point of −4 V using op-amps.

**Model Question**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

FIFTH SEMESTER B.TECH DEGREE EXAMINATION, (**Model Question Paper)**

**Course Code: ECT301**

**Program: Electronics and Communication Engineering**
**Course Name: Linear Integrated Circuits**

Max. Marks: 100 Duration: 3 Hours

**PART A**

Answer ALL Questions. Each Carries 3 mark.

| | | |
|---|---|---|
| 1. | Draw and list the functions of 741 IC pins | K1 |
| 2. | Define slew rate with its unit. What is its effect at the output signal? | K2 |
| 3. | How the virtual ground is different from actual ground? | K2 |
| 4. | A differential amplifier has a common mode gain of 0.05 and difference mode gain of 1000.Calculate the output voltage for two signals V1 = 1mV and V2 = 0.9Mv | K3 |
| 5. | Design a non-inverting amplifier for a gain of 11 | K3 |
| 6. | Design a second order Butterworth Low Pass Filter with $f_H$= 2KHz | K3 |
| 7. | Draw the circuit of monostable multivibrator using opamp. | K1 |
| 8. | What is the principle of VCO?. | K1 |
| 9. | Mention 3 applications of PLL. | K2 |
| 10. | Define the following terms with respect to DAC (i)Resolution (ii)Linearity (iii) Full scale output voltage | K2 |
| | Differentiate between line and load regulations. | K3 |

**PART – B**

Answer one question from each module; each question carries 14 marks.

| | | | | |
|---|---|---|---|---|
| | **Module I** | | | |
| 11. a) | Derive CMRR, input resistance and output resistance of a dual input balanced output differential amplifier configuration. | 7 | CO1 | K3 |
| 11. b) | What is the principle of operation of Wilson current mirror and its advantages? Deduce the expression for its current gain. | 7 | CO1 | K2 |
| | **OR** | | | |
| 12.a) | Draw the equivalent circuit of an operational amplifier. Explain voltage transfer characteristics of an operational amplifier. | 6 | CO1 | K3 |
| 12.b) | Explain the following properties of a practical opamp (i) Bandwidth (ii) Slew rate (iii) Input offset voltage (iv) Input offset current | 8 | CO1 | K2 |
| | **Module II** | | | |

| | | | | |
|---|---|---|---|---|
| 13. a) | Design a fullwave rectifier to rectify an ac signal of 0.2V peak-to-peak. Explain its principle of operation. | 7 | CO2 | K3 |
| 13. b) | Draw the circuit diagram of a differential instrumentation amplifier with a transducer bridge and show that the output voltage is proportional to the change in resistance. | 7 | CO2 | K2 |
| | **OR** | | | |
| 14.a) | Derive the following characteristics of voltage shunt amplifier:<br>i) Closed loop voltage gain ii)Input resistance<br>iii) Output resistance iv)Bandwidth | 7 | CO2 | K3 |
| 14.b) | Explain the working of an inverting Schmitt trigger and draw its transfer characteristics. | 7 | CO2 | K2 |
| | **Moduel III** | | | |
| 15 a) | Derive the equation for frequency of oscillation (f0) of a Wein Bridge oscillator. Design a Wein Bridge oscillator for f0 = 1KHz. | 7 | CO3 | K3 |
| 15 b) | Derive the equation for the transfer function of a first order wide Band Pass filter. | 7 | CO3 | K3 |
| | **OR** | | | |
| 16a | Derive the design equations for a second order Butterworth active low pass filter. | 7 | CO3 | K3 |
| 16b | Design a circuit to generate 1KHz triangular wave with 5V peak. | 7 | CO3 | K3 |
| | **Module IV** | | | |
| 17 a) | Design a circuit to multiply the incoming frequency by a factor of 5 using 565 PLL. | 8 | CO4 | K3 |
| 17 b) | With the help of internal diagram explain the monostable operation of timer IC 555. Draw the input and output waveforms. Derive the equation for pulse width. | 6 | CO4 | K2 |
| | **OR** | | | |
| 18 a) | Design a monostable multi-vibrator for a pulse duration of 1ms using IC555. | 7 | CO4 | K3 |
| 18 b) | Explain the operation of Phase Locked Loop. What is lock range and capture range? | 7 | CO4 | K2 |
| | **Module V** | | | |
| 19 a) | Explain the working of R-2R ladder type DAC. In a 10 bit DAC, reference voltage is given as 15V. Find analog output for digital input of 1011011001. | 7 | CO5 | K2 |
| 19 b) | Explain how short circuit, fold back protection and current boosting are done using IC723 voltage regulator. | 7 | CO5 | K2 |
| | **OR** | | | |
| 20 a) | With a functional diagram, explain the principle of operation of Successive approximation type ADC. | 7 | CO5 | K2 |
| 20 b) | With a neat circuit diagram, explain the operation of a 3-bit flash converter. | 7 | CO5 | K2 |

| EVT 303 | FPGA BASED SYSTEM DESIGN | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:** This course aims to develop the skill of FPGA based system design.

**Prerequisite:** ECT203 Logic Circuit Design.

**Course Out Comes: A**fter the completion of the course the student will be able to:

| | |
|---|---|
| **CO1** | Design simple digital systems with programmable logic devices. |
| **CO2** | Analyze the features, limitations, and architectures of various programmable logic devices and implement medium-scale integration (MSI) circuits using appropriate PLDs. |
| **CO3** | Analyze the architecture of FPGA. |
| **CO4** | Analyze the design considerations of FPGA. |
| **CO5** | Understand the features and architecture of commercial FPGAs, implement basic digital circuits, and utilize IP core integration, High-Level Synthesis, and on-chip debugging tools in FPGA design. |

## Mapping of course outcomes with program outcomes:

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO2** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO3** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO4** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO5** | 3 | 3 | | | 2 | | | | | | | 2 |

**Assessment Pattern:**

| Bloom's Category | | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|---|
| | | 1 | 2 | |
| Remember | K1 | 10 | 10 | 20 |
| Understand | K2 | 20 | 20 | 40 |
| Apply | K3 | 10 | 10 | 20 |
| Analyse | K4 | 10 | 10 | 20 |
| Evaluate | | | | |
| Create | | | | |

## Mark distribution:

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 Hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks

Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern**

**Maximum Marks: 100** **Time: 3 hours**

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 subdivisions and carry 14 marks.

## Course Level Assessment Questions

**Course Outcome 1 (CO1**): Design simple digital systems with programmable logic devices.

1. Explain the trade-offs between different digital system design approaches such as ASIC, FPGA, and microcontroller-based solutions. Provide examples of applications where each would be preferable.
2. Using Verilog HDL, design a finite state machine (FSM) for a simple traffic light controller. Include the state diagram, Verilog code, and a testbench to simulate its functionality.
3. Given a Verilog model of a combinational circuit, identify synthesis issues such as latches, non-synthesizable constructs, and race conditions. Propose modifications to ensure the design is synthesizable and reliable.

**Course Outcome 2 (CO2):**

1. Compare the architectures and functionalities of ROM, PLA, PAL, CPLD, and FPGA. Discuss their relative advantages and limitations for implementing digital logic. Explain the architecture of logic block of FPGA.
2. Design and implement a 4-to-1 multiplexer and a 2-bit binary counter using a suitable programmable logic device. Justify your choice of PLD and provide the implementation steps.
3. Given a medium-scale integration (MSI) circuit function (e.g., a BCD to 7-segment decoder), explain how it can be implemented using a CPLD or FPGA. Discuss the resource utilization and programming approach involved.

**Course Outcome 3 (CO3):**

1. Differentiate between coarse-grained and fine-grained FPGA architectures. Discuss how granularity affects design flexibility, performance, and resource utilization. Analyze Timing and Power dissipation in a typical FPGA.
2. Analyze the logic block and I/O block architectures of Xilinx and Altera FPGAs. How do vendor-specific features influence timing performance and power dissipation?
3. Given the specifications of an FPGA logic cell and I/O block, estimate the timing delays and power dissipation for implementing a 4-bit shift register. Justify your assumptions based on typical FPGA architectural parameters.

**Course Outcome 4 (CO4):**

1. Explain the role of partitioning and placement in the FPGA design flow. How do these steps impact overall design performance and routing complexity?
2. Analyze the impact of routing resource limitations and interconnect delays on the timing closure of a complex FPGA design. Propose strategies to mitigate these challenges.

3. Design a simple digital signal processing (DSP) module or embedded system component using an FPGA. Describe how placement and routing considerations influence your design choices and performance outcomes.

**Course Outcome 5 (CO5):**

1. Compare the key features and architectural differences of Xilinx, Altera, and Actel FPGA families, including the Zynq-7000 SoC. Highlight the applications suited for each series.

2. Using Vivado, implement a simple sequential circuit (e.g., a 4-bit counter) on a Xilinx Virtex FPGA. Integrate an IP core and explain the steps involved in its configuration and reuse.

3. Describe the workflow of High-Level Synthesis (HLS) using Vivado HLS. How can on-chip debugging tools like the Integrated Logic Analyzer (ILA) be used to validate and optimize FPGA designs?

## Syllabus

| Module | Course contents |
|---|---|
| I | Introduction: Digital system design options and tradeoffs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioral modelling and simulation, Hardware description languages (emphasis on Verilog), combinational and sequential design, state machine design, synthesis issues, test benches. |
| II | Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Limitations, Architectures and Programming. Implementation of MSI circuits using Programmable logic Devices. |
| III | FPGA architecture: FPGA Architectural options, granularity of function and wiring resources, coarse V/s fine grained, vendor specific issues (emphasis on Xilinx and Altera), Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation. |
| IV | Placement and Routing: Programmable interconnect - Partitioning and Placement, Routing resources, delays; Applications -Embedded system design using FPGAs, DSP using FPGAs. |

| | |
|---|---|
| **V** | Commercial FPGAs: Xilinx, Altera, Actel (Different series description only), Zynq 7000 SoC, Features, Basic Block diagram, Case study Xilinx, Virtex: implementation of simple combinational and sequential circuits. IP Core Integration and Reuse: Overview of IP cores and IP catalog in FPGA tools, High-Level Synthesis (HLS) and Vivado HLS, On-chip debugging tools (e.g., ILA - Integrated Logic Analyzer). |

**Text Books:**


1. FPGA-Based System Design Wayne Wolf, Verlag: Prentice Hall
2. Modern VLSI Design: System-on-Chip Design (3rd Edition) Wayne Wolf, Verlag


# References:


1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic
2. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall
3. Field programmable gate array, S. Brown, R.J. Francis, J. Rose, Z.G. Vranesic, 2007, BS.
4. Zynq -7000 SoC Technical Reference manual.


## Course Contents and Lecture Schedule

| No | Topic | No.of. Lectures |
|---|---|---|
| | **Module I** | |
| 1.1 | Introduction: Digital system design options and tradeoffs, Design methodology and technology overview. | **2** |
| 1.2 | High Level System Architecture and Specification: Behavioral modelling and simulation. | **2** |
| 1.3 | Hardware description languages (emphasis on Verilog). | |

| | | |
|---|---|---|
| | | |
| 1.4 | combinational and sequential design | **2** |
| 1.5 | state machine design | **2** |
| 1.6 | synthesis issues, test benches. | **1** |
| | TUTORIAL | **1** |
| **Module II** | | |
| 2.1 | Programmable logic Devices: ROM, PLA, PAL Features, | **2** |
| 2.2 | Programmable logic Devices: CPLD, FPGA Features, Limitations, | **1** |
| 2.3 | Architectures and Programming. Implementation of MSI circuits using Programmable logic Devices. | **2** |
| | TUTORIAL | **2** |
| **Module III** | | |
| 3.1 | FPGA architecture: FPGA Architectural options, granularity of function and wiring resources. | **2** |
| 3.2 | coarse V/s fine grained | **1** |
| 3.3 | vendor specific issues (emphasis on Xilinx and Altera clock input). | **1** |
| 3.4 | Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics. | **2** |
| 3.5 | Timing, Power dissipation. | **1** |
| | TUTORIAL | **2** |
| **Module IV** | | |
| 4.1 | Placement and Routing: Programmable interconnect - Partitioning and Placement. | **1** |
| 4.2 | Routing resources, delays. | **1** |
| 4.3 | Applications -Embedded system design using FPGAs, DSP using FPGAs. | **2** |
| | TUTORIAL | **2** |

| Module V | | |
|---|---|---|
| 5.1 | Commercial FPGAs: Xilinx, Altera, Actel (Different series description only), Zynq 7000 SoC, Features, Basic Block Diagram | **1** |
| 5.2 | Case study Xilinx Virtex: implementation of simple combinational and sequential circuits. | **1** |
| 5.3 | IP Core Integration and Reuse: Overview of IP cores and IP catalog in FPGA tools | **1** |
| 5.4 | High-Level Synthesis (HLS) and Vivado HLS, On-chip debugging tools (e.g., ILA - Integrated Logic Analyzer). | **1** |
| 5.4 | TUTORIAL | **1** |

# Model Question paper

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

FIFTH SEMESTER B. TECH DEGREE EXAMINATION

## Course Code: EVT 302

**Course Name: FPGA BASED SYSTEM DESIGN**

Max. Marks:100 Duration: 3 Hours

**PART A**

**(*Answer All Questions*)**

| | | |
|---|---|---|
| 1 | Design a half adder using PAL. | (3) |
| 2 | What is meant by a CLB? Explain. | (3) |
| 3 | Draw the general architecture of Altera FPGA. | (3) |
| 4 | Compare coarse- and fine-grained FPGA architecture. | (3) |
| 5 | Give an example for base function | (3) |
| 6 | List the various steps involved in design verification | (3) |
| 7 | Explain energy strategy of routing in FPGA | (3) |
| 8 | What are the benefits of FPGA in DSP design | (3) |
| 9 | List different commercially available FPGA'S | (3) |
| 10 | How do you implement a sequential circuit on FPGA | (3) |

**PART B**

**(*Answer one question from each module. Each question carries 14 marks*) MODULE I**

| | | |
|---|---|---|
| 11 a) | Write the Verilog code for a 4:1 multiplexer using behavioral model. Write truth table also draw schematic. | (8) |

b) Write the test bench of 4:1 multiplexer using Verilog. (6)

**OR**

12a) Design a full subtractor and write behavioral level coding using verilog (7)

b) What is Mealy model. (7)

## MODULE II

13 a) Implement the following Boolean expressions using a suitable PLA (9)

$A(x,y,z) = \sum m(1,2,4,6)$. $B(x,y,z) = \sum m(0,1,6,7)$.

$C(x,y,z) = \sum m(2,6)$. $D(x,y,z) = \sum m(1,2,3,5,7)$.

b) Compare CPLD and FPGA 6)

**OR**

14 a) Comparison between PROM, PLA, PAL. (7)

b) Draw the structure of ROM and explain it.

(7)

## Module III

15 With neat diagram explain the internal architecture of FPGA.

(14)

OR

16 a) Explain logic block with neat diagram (7)

b) Draw and explain I/O block architecture of FPGA (7)

**Module IV**

17 a) Explain in detail three major classes of placement in FPGA. (10)

b) Explain the placement issues in FPGA (4)

**OR**

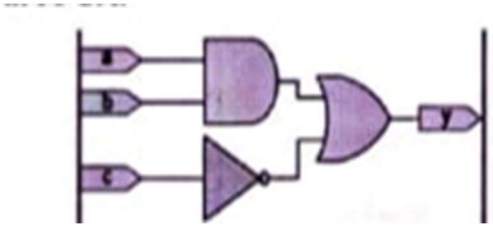
18 a) With neat diagram explain different programmable inter connections in FPGA. (7)

b) Explain FPGA Routing Techniques (7)

**MODULE V**

19 a) What is LUT in FPGA. Design and implement the following combinational circuit using LUT s in FPGA.

7



19 b) Explain with diagram, how to implement an 8 bit adder using 8 bit LUTs and 4 bit LUTs 7

**OR**

20) With neat diagram explain the architecture of Xilinx Virtex. (14 )

| EVT 305 | DIGITAL CMOS DESIGN | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:** This course aims to develop the knowledge and analytical skills required for designing and analyzing CMOS digital circuits. The student will gain knowledge in the operation of MOS transistors.

**Prerequisites:** ECT 201 Solid State Devices, ECT 203 Logic Circuit Design.

**Course Out Comes: A**fter the completion of the course the student will be able to:

| | |
|---|---|
| **CO1** | Understand the basic operation of MOSFET and CMOS Inverter. |
| **CO2** | Design basic CMOS Digital Circuits. |
| **CO3** | Design various types of Static and Dynamic Digital CMOS Circuits. |
| **CO4** | Design Combinational and Sequential circuit using CMOS logic. |
| **CO5** | Design CMOS Data Path Subsystems |

**Mapping of course outcomes with program outcomes:**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO2** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO3** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO4** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO5** | 3 | 3 | | | 2 | | | | | | | 2 |

**Assessment Pattern:**

| Bloom's Category | | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|---|
| | | 1 | 2 | |
| Remember | K1 | 10 | 10 | 20 |
| Understand | K2 | 20 | 20 | 40 |
| Apply | K3 | 10 | 10 | 20 |
| Analyse | K4 | 10 | 10 | 20 |
| Evaluate | | | | |
| Create | | | | |

**Mark distribution:**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 Hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern**

**Maximum Marks: 100** **Time: 3 hours**

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum of 2 subdivisions and carry 14 marks.

**Course Level Assessment Questions**
**Course Outcome 1 (CO1):**

1. Explain the structure and operation of MOSFETs.
2. Explain the condition for strong inversion in a MOS structure.
3. Plot the I -V characteristics of long channel MOSFETs.
4. Draw and explain simple MOS capacitance model.
5. Explain the short channel effects in MOSFET devices.
6. Sketch the voltage transfer characteristics of CMOS inverter.
7. Describe the operation of CMOS inverter.
8. Sketch the load inverter characteristics.

**Course Outcome 2 (CO2):**

1. Implement the given expression using static CMOS logic, z=(D+E+A)(B+C)'.
2. Implement an XNOR circuit using pseudo NMOS logic.
3. Determine the limitation of dynamic CMOS circuits. Formulate a suitable design to overcome the issue.
4. Implement the function z=AB+(C+D)(E+F)+GH using domino CMOS logic.
5. Describe NP domino logic with necessary diagrams.

**Course Outcome 3 (CO3):**

1. What is ratioed logic, and how does it differ from fully complementary logic?
2. Describe the concept and operation of pseudo NMOS logic.
3. How does the aspect ratio of transistors affect the performance of ratioed logic gates?
4. What is pass transistor logic, and how is it different from traditional CMOS logic?
5. Describe the structure and operation of a DCVS gate.

6. What is differential pass transistor logic?
7. Provide an example of a circuit designed using differential pass transistor logic.
8. What is transmission gate logic, and how does it operate?
9. How does dynamic CMOS logic differ from static CMOS logic?
10. What is clock feedthrough, and how does it affect dynamic circuits?
11. What is Domino logic, and how does it work in dynamic CMOS design?
12. Compare the performance of Domino CMOS logic and NP Domino CMOS logic with suitable example.

**Course Outcome 4 (CO4):**

1. Explain True Single-Phase Clocked register (TRSPCR)
2. Compare the Clocked CMOS and TSPC latch circuits.
3. With the help of circuit diagram explain the operation of full CMOS SRAM cell.
4. Design a 1T DRAM cell and show its Read and Write Operation.
5. Explain the operation of 6T SRAM cell.
6. Explain read/write operation of SRAM memory cell. How 1 bit cell is used in bigger memory systems.

**Course Outcome 5(CO5):**

1. Explain the working of carry bypass adder and obtain the expression for worst case delay.
2. Explain the operation of array multiplier.
3. What are the advantages and disadvantages of carry-bypass adders?
4. How does a linear carry-select adder improve addition speed?
5. How does the square-root carry-select adder achieve faster addition times?
6. How do partial products get generated and summed in an array multiplier?

## Syllabus

| Module | Course contents | Hours |
|---|---|---|
| I | MOS transistor: MOS structure, MOS system under external bias , Structure and operation of MOSFETs, Threshold voltage, Long channel I-V characteristics, CV characteristic- simple MOS capacitance model, detailed MOS gate capacitance model, , Non ideal IV effects - mobility degradation and velocity saturation, Channel length modulation, threshold voltage effects -body effect, DIBL, short channel effects. | |
| II | The MOS Inverter: Principle, static characteristics - Voltage Transfer characteristics, Logic threshold, Noise immunity and Noise margins, Depletion and enhancement load inverters (only quantitative analysis needed) CMOS Inverter: - circuit operation, design of CMOS inverter, Noise margin- Calculation, Supply voltage scaling. | |
| III | Designing Combinational logic gates in CMOS: Static CMOS design- Basic concepts and properties, Realization of simple gates, Fully Complementary logic, Ratioed logic - NMOS and Pseudo NMOS logic, Pass transistor logic, Differential cascode voltage switch logic (DCVS), Differential pass transistor logic, Transmission gate logic. Dynamic CMOS logic design - Basic concepts and properties, Dynamic gates - signal integrity issues in dynamic design - charge leakage, charge sharing, capacitive coupling, clock feed through, cascading dynamic gates - Domino logic - NP Domino. | |

| | |
|---|---|
| **IV** | Designing sequential circuits, Static latches and Registers, Multiplexer based latches - Master Slave edge triggered register using Mux, Dynamic latches and registers - Dynamic transmission gate edge triggered registers, $C^2$MOS Registers, True Single Phase Clocked Register (TSPCR), Designing memory - Memory classification - Memory architecture and building blocks, Read only memory - 4 x 4 MOS ROM Cell arrays (OR, NOR, NAND), Random Access Memory - SRAM, Six transistor CMOS RAM cell, DRAM - Three transistor and one transistor Dynamic memory cell. |
| **V** | Data paths in Digital Processor Architecture, Adder- Definition, Full adder circuit design consideration - Static adder, Binary adder - Logic design considerations, Carry-bypass adder, Linear carry select adder, Square-root carry-select adder, Multiplier - Array multiplier. |

**Text Books:**

1. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.

2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", Tata MGH, 3rd edition.2003.

3. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Pearson Education, Second, Edition, 2003.

**Course Contents and Lecture Schedule.**

| No | Topic | No.of. Lectures |
|---|---|---|
| | **Module I** | |
| 1.1 | MOS transistor: MOS structure, MOS system under external bias, Structure and operation of MOSFETs, Threshold voltage, Long channel I-V characteristics. | **4** |
| 1.2 | CV characteristic- simple MOS capacitance model, detailed MOS gate capacitance model | **4** |
| 1.3 | Non ideal IV effects - mobility degradation and velocity saturation, Channel length modulation, threshold voltage effects -body effect, DIBL, short channel effects. | |
| | TUTORIAL | **1** |
| | **Module II** | |
| 2.1 | The MOS Inverter: Principle static characteristics - Voltage Transfer characteristics, Logic threshold. | **3** |
| 2.2 | Noise immunity and Noise margins, Depletion and enhancement load inverters (only quantitative analysis needed) | **3** |
| 2.3 | CMOS Inverter: - circuit operation, design of CMOS inverter, Noise margin-Calculation, Supply voltage scaling. | **3** |
| | TUTORIAL | **2** |

| | | |
|---|---|---|
| | **Module III** | |
| | | |
| 3.1 | Designing Combinational logic gates in CMOS: Static CMOS design- Basic concepts and properties, Realization of simple gates, Fully Complementary logic, | **2** |
| 3.2 | Ratioed logic - NMOS and Pseudo NMOS logic, Pass transistor logic, Differential cascode voltage switch logic (DCVS), Differential pass transistor logic, Transmission gate logic. | **1** |
| 3.3 | Dynamic CMOS logic design - Basic concepts and properties, Dynamic gates - signal integrity issues in dynamic design - charge leakage, charge sharing, capacitive coupling, clock feed through, cascading dynamic gates | **1** |
| 3.4 | Domino logic - NP Domino. | **2** |
| | TUTORIAL | **2** |
| | **Module IV** | |
| 4.1 | Designing sequential circuits, Static latches and Registers, Multiplexer based latches - Master Slave edge triggered register using Mux. | **1** |
| 4.2 | Dynamic latches and registers - Dynamic transmission gate edge triggered registers. | **1** |
| 4.3 | $C^2$MOS Registers, True Single Phase Clocked Register (TSPCR). | **2** |
| 4.4 | Designing memory - Memory classification - Memory architecture and building blocks. | **1** |
| 4.5 | Read only memory - 4 x 4 MOS ROM Cell arrays (OR, NOR, NAND), Random Access Memory - SRAM, Six transistor CMOS RAM cell. | **2** |
| 4.6 | DRAM - Three transistor and one transistor Dynamic memory cell. | 2 |
| | TUTORIAL | **2** |
| | **Module V** | |
| 5.1 | Data paths in Digital Processor Architecture, Adder- Definition, Full adder circuit design consideration - Static adder, | **2** |
| 5.2 | Binary adder - Logic design considerations, Carry-bypass adder, Linear carry select adder, Square-root carry-select adder, | **3** |
| 5.3 | Multiplier - Array multiplier. | **1** |
| | TUTORIAL | **2** |

**Model Question paper**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

FIFTH SEMESTER B. TECH DEGREE EXAMINATION

**Course Code:**

**Course Name: DIGITAL CMOS DESIGN**

Max. Marks:100 Duration: 3 Hours

**PART A**

**(*Answer All Questions*)**

1. Describe the three regions of operation of MOS transistor. (3)
2. Explain a simple MOS capacitance model. (3)
3. Explain 2 Input NOR gate with depletion NMOS loads. Calculate output high voltage and output low voltage? (3)
4. Consider a CMOS inverter circuit with following parameters: VDD=3.3V, VTO.N=0.6V, VTO.P=0.7V, Kn=200uA/V^2 , Kp=80uA/V^2. Calculate noise margins of circuit. (3)
5. Develop 2 Input NOR gate by Pseudo NMOS Logic and perform its functional verification by using a functional verification table. (3)
6. Sketch the complementary pass transistor logic implementation of a NAND2. (3)
7. Classify semiconductor memories. (3)
8. Compare SRAM and DRAM. (3)
9. What techniques can be used to optimize the speed of full adders? (3)
10. List the advantages of carry select adder. (3)

**PART B**

**(*Answer one question from each module. Each question carries 14 marks*)**

**MODULE I**

11. a) Summarize the Short channel effects in MOS transistors. (6)

b) In the circuit below, assume $(W/L)_1 = 50/0.5$, $R_D = 2k\Omega$ and $\lambda = 0$. (8)

(I) What is the small signal gain if $M_1$ is in saturation and ID = 1mA?

(II) What input voltage places $M_1$ at the edge of the triode region? What is the small signal gain under this condition?

**OR**

12. a) Describe the Level 1 and Level 2 MOS device model. (7)

b) Calculate the diffusion parasitic Cdb of the drain of a unit-sized contacted nMOS transistor in a 65 nm process when the drain is at 0 V and the drain is at VDD = 1.0 V. Assume the substrate is grounded. The diffusion region conforms to the design rules with $\lambda$ = 25 nm. The transistor characteristics are CJ = 1.2 fF/um2, MJ = 0.33, CJSW = 0.1 fF/μm, CJSWG = 0.36 fF/μm, MJSW = MJSWG = 0.10, and $\Psi 0$ = 0.7 V at room temperature. (7)

**MODULE 2**

13 a) Define Threshold Voltage (VTH). Discuss the dependency of VTH on various parameters. Explain the DC noise margin of CMOS logic. (7)

b) Explain in detail about voltage transfer characteristics of CMOS Inverter. (7)

**OR**

14 a) Derive expression for VOL, VOH ,VIL & VIH of CMOS inverter. (7)

b) Explain and derive the necessary DC region equations of a CMOS inverter. (7)

**MODULE 3**

**15** a) Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions: (7)

a) $Y = \overline{ABC + D}$

b) $Y = \overline{(AB + C) \cdot D}$

c) $Y = \overline{AB + C \cdot (A + B)}$

b) )Discuss the signal integrity issues in dynamic design. (7)

**OR**

**16** a) Develop a 2 X 1 Multiplexer using Transmission gates and interpret its operation using different input combinations. (7)

b) Explain the benefits of Domino CMOS. (7)

**MODULE 4**

17 a) Summarize the operation of , $C^2$MOS Registers. (7)

b) Draw the circuit diagram of True Single Phase Clocked Register (TSPCR).What are its advantages. (7)

**OR**

18a) Draw the circuit diagram of a 6T SRAM cell. How are the READ/WRITE operations performed in an SRAM cell? (10)

b) Differentiate between static latches and dynamic latches. (4)

**MODULE 5**

19 a) Describe the structure and operation of a basic array multiplier (8)

b) Describe how arithmetic and logic units (ALUs) are integrated into data paths. (6)

**OR**

20 a) Draw the configuration of a square root carry select adder and mark its worst case signal arrival time. What are its advantages?. (10)

b) Explain the concept of logic design in the context of adders. (4)

| EVT 307 | VLSI TECHNOLOGY | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:** This course aims to understand the basic steps of fabrication.

**Prerequisite:** ECT 201 Solid State Devices

**Course Out Comes: A**fter the completion of the course the student will be able to:

| | |
|---|---|
| **CO1** | Understand the fundamentals of IC fabrication |
| **CO2** | Explain lithography and mask generation techniques, evaluate advanced lithographic methods and processing technologies, and understand their applications in ULSI, bipolar, and NMOS circuit fabrication. |
| **CO3** | Apply etching techniques to achieve precise pattern transfer in semiconductor manufacturing. Identify suitable diffusion, ion implantation, and etching techniques for specific applications in semiconductor manufacturing. |
| **CO4** | Identify suitable thin film deposition techniques for specific applications in semiconductor manufacturing, electronics, optics, and materials science. |
| **CO5** | Understand the design rules for NMOS and CMOS technologies and their importance in ensuring manufacturability and reliability. |

**Mapping of course outcomes with program outcomes:**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO2** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO3** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO4** | 3 | 3 | | | 2 | | | | | | | 2 |
| **CO5** | 3 | 3 | | | 2 | | | | | | | 2 |

**Assessment Pattern:**

| Bloom's Category | | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|---|
| | | 1 | 2 | |
| Remember | K1 | 10 | 10 | 20 |
| Understand | K2 | 20 | 20 | 40 |
| Apply | K3 | 10 | 10 | 20 |
| Analyse | K4 | 10 | 10 | 20 |
| Evaluate | | | | |
| Create | | | | |

**Mark distribution:**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 Hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern**

**Maximum Marks: 100** **Time: 3 hours**

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 subdivisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1):**

1. What are the primary applications of MEMS (Microelectromechanical Systems) technology?
2. Describe the fabrication process of a basic MEMS device.
3. Explain the process of silicon crystal growth using the Czochralski method.
4. What is a clean room and why is it essential in semiconductor manufacturing?
5. How do you control the oxidation environment to achieve desired oxide thickness and quality?

**Course Outcome 2 (CO2):**

1. What are the different types of lithography used in semiconductor manufacturing?
2. What is a photomask and how is it used in the lithography process?
3. What is the role of optical aligners in the lithography process?
4. How do step-and-repeat aligners differ from step-and-scan aligners?
5. How can resolution enhancement techniques (RETs) improve lithography performance?
6. How does the depth of focus impact the lithographic process at smaller feature sizes?
7. How does X-ray lithography achieve higher resolution compared to optical lithography?
8. What are plasma processes, and how are they utilized in semiconductor fabrication?
9. What are the key differences between NMOS and CMOS technologies?
10. Describe the key steps involved in the fabrication of bipolar transistors.

**Course Outcome 3 (CO3):**

1. What is the difference between pre-deposition and drive-in diffusion in semiconductor fabrication?
2. What factors determine the junction depth in diffusion processes?
3. What are the limitations and problems associated with thermal diffusion?
4. What role do masks play in ion implantation?
5. Explain the energy loss mechanisms during ion implantation.
6. How is the depth profile of implanted ions determined?
7. Define range and straggle in the context of ion implantation.
8. What is ion channeling and how can it be minimized?
9. What is anisotropy in etching and why is it important for semiconductor fabrication?
10. Describe the differences between wet etching and plasma etching.
11. How does reactive ion etching (RIE) differ from plasma etching?

12. Discuss the factors that affect the etch rate and uniformity in reactive ion etching.

**Course Outcome 4 (CO4):**

1. What is Physical Vapor Deposition (PVD) and how does it work?.
2. Describe the process of thermal evaporation in PVD.
3. Describe the sputtering process and the differences between DC sputtering and RF sputtering.
4. Compare and contrast the advantages and disadvantages of CVD techniques over PVD techniques.
5. How does Plasma Enhanced CVD (PECVD) differ from conventional CVD techniques, and what advantages does it offer?
6. What are the common materials used in both PVD and CVD processes, and how do their properties influence the choice of deposition method?
7. How do substrate temperature and chamber pressure affect the deposition rate and film properties in both PVD and CVD processes?
8. What is Atmospheric Pressure CVD (APCVD) and in what scenarios is it typically used?
9. Describe the sputtering process and the differences between DC sputtering and RF sputtering

**Course Outcome 5 (CO5):**

1. What is the significance of the mask sequence in the fabrication of NMOS transistors?
2. Compare the process steps involved in silicon gate and metal gate NMOS transistor technologies.
3. What are the key limitations of NMOS technology in modern semiconductor manufacturing?
4. How does the lithography process utilize masks to define regions for doping and metallization in NMOS transistors?
5. Explain the role of design rule check (DRC) in ensuring compliance with design rules during the layout process.

**Syllabus**

| Module | Course contents | Hours |
|---|---|---|
| I | History of IC's; Operation & Models for Devices of Interest: CMOS and MEMS. Electronic Materials: Crystal Structures, Defects in Crystals, Si, Poly Si, Si Crystal Growth. Clean room and Wafer Cleaning: Definition, Need of Clean Room, RCA cleaning of Si.<br>Processes in Fabrication, - Oxidation, Dry and Wet Oxidation, Kinetics of Oxidation, Oxidation Rate Constants, Dopant Redistribution, Oxide Charges, Device Isolation, LOCOS, Oxidation System. | |
| II | Lithography and Mask generation techniques: Overview of Lithography, Radiation Sources, Masks, Photoresist, Components of Photoresist Optical Aligners, Resolution, Depth of Focus, Advanced Lithography: E-beam Lithography,X-ray Lithography, Ion Beam Lithography. Advanced Unit-Processors for ULSI Circuit Technologies., - Use of RTP, - Plasma processes in the fabrication in the fabrication of circuits., Basic Bipolar process Technologies., NMOS Technology . | |
| III | Pre-Deposition and Drive-in Diffusion Modeling, Dose, 2-Step Diffusions, Successive Diffusion, Lateral Diffusion, Series Resistance, Junction Depth, Irvin's Curves, Diffusion System.<br>Ion Implantation: Problems in Thermal Diffusion, Advantages of Ion Implantation, Applications in ICs, Ion Implantation System, Mask, Energy Loss Mechanisms, Depth Profile, Range & Straggle, Lateral Straggle, Dose, Junction Depth, Ion Implantation Damage, Post Implantation Annealing, Ion Channeling, Multi Energy Implantation.<br>Etching: Anisotropy, Selectivity, Wet Etching, Plasma Etching, Reactive Ion Etching. | |

| | |
|---|---|
| **IV** | Thin Film Deposition: Physical Vapor Deposition: Thermal evaporation, Resistive Evaporation, Electron beam evaporation, Laser ablation, Sputtering Chemical Vapor Deposition: Advantages and disadvantages of Chemical Vapor deposition (CVD) techniques over PVD techniques, reaction types,Boundaries and Flow, Different kinds of CVD techniques: APCVD, LPCVD, Metalorganic CVD(MOCVD), Plasma Enhanced CVD etc. |
| **V** | Mask sequence based fabrication process for NMOS transistors, - Silicon Gate and Metal Gate Technologies. Limitations of NMOS Technology.CMOS Technology - Process Sequence for CMOS Technology, Advanced CMOS Processes, ―Design Rules for NMOS and CMOS Technologies as ―Constraints for Layouts. |

**Text Books**


1. Silicon VLSI Technology, Plummer, Deal and Griffin ,1st Edition, Pearson Education,2009
2. Fundamental of Semiconductor Fabrication, Sze and May,2nd Edition, Wiley India, 2009
3. Silicon Process Technology, S K Gandhi,2nd Edition, Wiley India,2009
4. VLSI Fabrication principles S.K. Ghandhi, , John Wiley Inc., New York, 1983
5. VLSI Technology S.M. Sze, 2nd Edition, McGraw Hill Co. Inc., New York, 1988
6. VLSI Technology C. Y. Chang and S. M. Sze, ― ‖, McGraw Hill Co. Inc., New York, 1996


**Course Contents and Lecture Schedule.**

| No | Topic | No.of. Lectures |
|---|---|---|
| | **Module I** | |
| 1.1 | History of IC's; Operation & Models for Devices of Interest: CMOS and MEMS. | **2** |
| 1.2 | Electronic Materials: Crystal Structures, Defects in Crystals, Si, Poly Si | **2** |
| 1.3 | Si Crystal Growth. Clean room and Wafer Cleaning: Definition, Need of Clean Room, RCA cleaning of Si. | |
| 1.4 | Processes in Fabrication, - Oxidation, Dry and Wet Oxidation, Kinetics of Oxidation, Oxidation Rate Constants | **2** |
| 1.5 | Dopant Redistribution, Oxide Charges. | **2** |
| 1.6 | Device Isolation, LOCOS, Oxidation System | **1** |
| | TUTORIAL | **1** |
| | **Module II** | |
| 2.1 | Lithography and Mask generation techniques: Overview of Lithography, Radiation Sources, Masks, Photoresist, Components of Photoresist Optical Aligners, Resolution, Depth of Focus | **2** |
| 2.2 | Advanced Lithography: E-beam Lithography,X-ray Lithography, Ion Beam Lithography. | **2** |
| 2.3 | Advanced Unit-Processors for ULSI Circuit Technologies., - Use of RTP, - plasma processes in the fabrication in the fabrication of circuits., Basic Bipolar process Technologies., NMOS Technology | **2** |
| | TUTORIAL | **2** |

| Module III | | |
|---|---|---|
| 3.1 | Pre-Deposition and Drive-in Diffusion Modeling, Dose | **2** |
| 3.2 | 2-Step Diffusions, Successive Diffusion, Lateral Diffusion, Series Resistance, Junction Depth, Irvin's Curves, Diffusion System. | **2** |
| 3.3 | Ion Implantation: Problems in Thermal Diffusion, Advantages of Ion Implantation, Applications in ICs, Ion Implantation System, Mask | **2** |
| 3.4 | Energy Loss Mechanisms, Depth Profile, Range & Straggle, Lateral Straggle, Dose, Junction Depth, Ion Implantation Damage, Post Implantation Annealing, Ion Channeling, Multi Energy Implantation. | **2** |
| 3.5 | Etching: Anisotropy, Selectivity, Wet Etching, Plasma Etching, Reactive Ion Etching. | **2** |
| | TUTORIAL | **2** |
| **Module IV** | | |
| 4.1 | Thin Film Deposition: Physical Vapor Deposition | **1** |
| 4.2 | Thermal evaporation, Resistive Evaporation, Electron beam evaporation, | **1** |
| 4.3 | Laser ablation, Sputtering Chemical Vapor Deposition: Advantages and disadvantages of Chemical Vapor deposition (CVD) techniques over PVD techniques. | **3** |
| 4.4 | Reaction types. Boundaries and Flow, | **1** |
| 4.5 | Different kinds of CVD techniques: APCVD, LPCVD, Metalorganic CVD(MOCVD), Plasma Enhanced CVD etc. | **2** |
| | TUTORIAL | **2** |
| **Module V** | | |
| 5.1 | Mask sequence based fabrication process for NMOS transistors, - Silicon Gate and Metal Gate Technologies. | **1** |
| 5.2 | Limitations of NMOS Technology.CMOS Technology - Process Sequence for CMOS Technology. | **1** |
| 5.3 | Advanced CMOS Processes, —Design Rules for NMOS and CMOS Technologies as —Constraints for Layouts | **2** |
| | TUTORIAL | **2** |

**Model Question paper**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

FIFTH SEMESTER B. TECH DEGREE EXAMINATION

**Course Code:**

**Course Name: VLSI TECHNOLOGY**

Max. Marks:100 Duration: 3 Hours

1. How do point defects and dislocations affect the properties of crystalline materials? (3)
2. Explain the RCA cleaning process for silicon wafers. (3)
3. Differentiate between positive and negative photoresist. (3)
4. What applications are best suited for ion beam lithography? (3)
5. How are Irvin's curves used to analyze doping profiles. (3)
6. Discuss the advantages of ion implantation over thermal diffusion. (3)
7. What is laser ablation and in what applications is it most useful?(3)
8. What are the safety and environmental concerns associated with each CVD technique, and how are they mitigated? (3)
9. How do issues such as power consumption and scaling challenges affect the performance of NMOS transistors? (3)
10. Explain the advantages and disadvantages of using metal gate technology over silicon gate technology in NMOS transistors (3)

**PART B**

***(Answer one question from each module. Each question carries 14 marks*)**

**MODULE I**

11 a) What are the main differences between dry and wet oxidation processes? (3)
b) How does the oxidation rate vary with temperature and pressure? (4)
c) Describe the kinetics of silicon oxidation and the role of oxidation rate constants. (7)

**OR**

12 a) What is the purpose of device isolation in semiconductor fabrication? (3)
b) Describe the LOCOS (Local Oxidation of Silicon) process and its advantages. (4)
c) Explain the concept of oxide charges and their impact on device performance. (7)

**MODULE II**

13 a) Describe the basic steps involved in the lithography process. (7)
b) Compare and contrast UV, DUV, and EUV lithography. (7)

**OR**

14 a) What is Rapid Thermal Processing (RTP) and why is it used in semiconductor fabrication? (7)
b) Describe the role of plasma etching in the fabrication of integrated circuits. (7)

## MODULE III

15 a) Describe the two-step diffusion process and its advantages. (7)

b) How does series resistance affect the performance of semiconductor devices? (7)

**OR**

16 a) Describe the components and operation of an ion implantation system. (7)

b) What is lateral straggle and how does it impact device performance? (7)

## MODULE IV

17 a) Explain the different types of chemical reactions involved in CVD processes. (7)

b) Explain the Low Pressure CVD (LPCVD) process and its benefits over APCVD. (7)

**OR**

18 a) What is Metalorganic CVD (MOCVD) and what are its specific applications in semiconductor manufacturing? (7)

b) Compare the film qualities and applications of APCVD, LPCVD, MOCVD, and PECVD. (7)

## MODULE V

19 a) Describe the complete process sequence for CMOS technology, starting from well formation to metallization. (8)

b) What are the advantages of FinFET technology over traditional planar CMOS transistors? (6)

**OR**

20 a) Describe the minimum feature sizes, spacing, and layer alignment requirements in NMOS and CMOS design rules. (7)

b) How does the use of high-k/metal gate integration enhance the performance of CMOS transistors? (7)

| HUT 300 | Industrial Economics & Foreign Trade | Category | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | HSMC | 3 | 0 | 0 | 3 |

**Preamble**: To equip the students to take industrial decisions and to create awareness of economic environment.

**Prerequisite**: Nil

**Course Outcomes**: After the completion of the course the student will be able to

| | |
|---|---|
| **CO1** | Explain the problem of scarcity of resources and consumer behaviour, and to evaluate the impact of government policies on the general economic welfare. (Cognitive knowledge level: **Understand**) |
| **CO2** | Take appropriate decisions regarding volume of output and to evaluate the social cost of production. (Cognitive knowledge level: **Apply**) |
| **CO3** | Determine the functional requirement of a firm under various competitive conditions. (Cognitive knowledge level: **Analyse**) |
| **CO4** | Examine the overall performance of the economy, and the regulation of economic fluctuations and its impact on various sections in the society. (Cognitive knowledge level: **Analyse**) |
| **CO5** | Determine the impact of changes in global economic policies on the business opportunities of a firm. (Cognitive knowledge level: **Analyse**) |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 2 | | | | | | | | | | 3 | |
| **CO2** | 2 | 2 | | | 2 | 2 | 3 | | | | 3 | |
| **CO3** | 2 | 2 | 1 | | | | | | | | 3 | |
| **CO4** | 2 | 2 | 1 | | | 1 | | | | | 3 | |
| **CO5** | 2 | 2 | 1 | | | | | | | | 3 | |

| Abstract POs defined by National Board of Accreditation | | | |
|---|---|---|---|
| **PO#** | **Broad PO** | **PO#** | **Broad PO** |
| PO1 | Engineering Knowledge | PO7 | Environment and Sustainability |
| PO2 | Problem Analysis | PO8 | Ethics |
| PO3 | Design/Development of solutions | PO9 | Individual and team work |
| PO4 | Conduct investigations of complex problems | PO10 | Communication |
| PO5 | Modern tool usage | PO11 | Project Management and Finance |
| PO6 | The Engineer and Society | PO12 | Lifelong learning |

**Assessment Pattern**

| **Bloom's Category** | **Continuous Assessment Tests** | | **End Semester Examination Marks** |
|---|---|---|---|
| | **Test 1 (Marks)** | **Test 2 (Marks)** | |
| Remember | **15** | **15** | **30** |
| Understand | **20** | **20** | **40** |
| Apply | **15** | **15** | **30** |

**Mark Distribution**

| **Total Marks** | **CIE Marks** | **ESE Marks** | **ESE Duration** |
|---|---|---|---|
| **150** | **50** | **100** | **3 hours** |

**Continuous Internal Evaluation Pattern:**

| | |
|---|---|
| Attendance | : 10 marks |
| Continuous Assessment - Test (2 numbers) | : 25 marks |
| Continuous Assessment - Assignment | : 15 marks |

**Internal Examination Pattern:**

Each of the two internal examinations has to be conducted out of 50 marks. First series test shall be preferably conducted after completing the first half of the syllabus and the second series test shall be preferably conducted after completing remaining part of the syllabus. There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly completed module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly completed module), each with 7 marks. Out of the 7 questions, a student should answer any 5.

**End Semester Examination Pattern:**

There will be two parts; Part A and Part B.

Part A : 30 marks

Part B : 70 marks

Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 3 sub-divisions and carries 14 marks.

## SYLLABUS

## HUT 300 Industrial Economics & Foreign Trade

### Module 1 (Basic Concepts and Demand and Supply Analysis)

Scarcity and choice - Basic economic problems- PPC – Firms and its objectives – types of firms – Utility – Law of diminishing marginal utility – Demand and its determinants – law of demand – elasticity of demand – measurement of elasticity and its applications – Supply, law of supply and determinants of supply – Equilibrium – Changes in demand and supply and its effects – Consumer surplus and producer surplus (Concepts) – Taxation and deadweight loss.

### Module 2 (Production and cost)

Production function – law of variable proportion – economies of scale – internal and external economies – Isoquants, isocost line and producer's equilibrium – Expansion path – Technical progress and its implications – Cobb-Douglas production function - Cost concepts – Social cost: private cost and external cost – Explicit and implicit cost – sunk cost - Short run cost curves - long run cost curves – Revenue (concepts) – Shutdown point – Break-even point.

### Module 3 (Market Structure)

Perfect and imperfect competition – monopoly, regulation of monopoly, monopolistic completion (features and equilibrium of a firm) – oligopoly – Kinked demand curve – Collusive oligopoly (meaning) – Non-price competition – Product pricing – Cost plus pricing – Target return pricing – Penetration pricing – Predatory pricing – Going rate pricing – Price skimming.

### Module 4 (Macroeconomic concepts)

Circular flow of economic activities – Stock and flow – Final goods and intermediate goods - Gross Domestic Product - National Income – Three sectors of an economy- Methods of measuring national income – Inflation- causes and effects – Measures to control inflation- Monetary and fiscal policies – Business financing- Bonds and shares -Money market and Capital market – Stock market – Demat account and Trading account - SENSEX and NIFTY.

### Module 5 (International Trade)

Advantages and disadvantages of international trade - Absolute and Comparative advantage theory - Heckscher - Ohlin theory - Balance of payments – Components – Balance of Payments

deficit and devaluation – Trade policy – Free trade versus protection – Tariff and non-tariff barriers.

**Reference Materials**


1. Gregory N Mankiw, 'Principles of Micro Economics', Cengage Publications
2. Gregory N Mankiw, 'Principles of Macro Economics', Cengage Publications
3. Dwivedi D N, 'Macro Economics', Tata McGraw Hill, New Delhi.
4. Mithani D M, 'Managerial Economics', Himalaya Publishing House, Mumbai.
5. Francis Cherunilam, 'International Economics', McGraw Hill, New Delhi.


**Sample Course Level Assessment Questions**

**Course Outcome 1 (CO1):**

1. Why does the problem of choice arise?
2. What are the central problems?
3. How do we solve the basic economic problems?
4. What is the relation between price and demand?
5. Explain deadweight loss due to the imposition of a tax.

**Course Outcome 2 (CO2):**

1. What is shutdown point?
2. What do you mean by producer equilibrium?
3. Explain break-even point;
4. Suppose a chemical factory is functioning in a residential area. What are the external costs?

**Course Outcome 3 (CO3):**

1. Explain the equilibrium of a firm under monopolistic competition.
2. Why is a monopolist called price maker?
3. What are the methods of non-price competition under oligopoly?

4. What is collusive oligopoly?

**Course Outcome 4 (CO4):**

1. What is the significance of national income estimation?
2. How is GDP estimated?
3. What are the measures to control inflation?
4. How does inflation affect fixed income group and wage earners?

**Course Outcome 5 (CO5):**

1. What is devaluation?
2. Suppose a foreign country imposes a tariff on Indian goods. How does it affect India's exports?
3. What is free trade?
4. What are the arguments in favour of protection?

**Model Question paper**

**QP CODE:** **PAGES:3**

**Reg No:_____** **Name :_____**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY FIFTH /SIXTH SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR**

**Course Code: HUT 300**

**Course Name: Industrial Economics & Foreign Trade**

**Max.Marks:100** **Duration: 3 Hours**

**PART A**

**Answer all Questions. Each question carries 3 Marks**

1. Why does an economic problem arise?
2. What should be the percentage change in price of a product if the sale is to be increased by 50 percent and its price elasticity of demand is 2?
3. In the production function $Q= 2L^{1/2}K^{1/2}$ if L=36 how many units of capital are needed to produce 60 units of output?
4. Suppose in the short run AVC 4. Suppose in the short run AVC<P<AC. Will this firm produce or shut down? Give reason.
5. What is predatory pricing?
6. What do you mean by non- price competition under oligopoly?
7. What are the important economic activities under primary sector?
8. Distinguish between a bond and share?
9. What are the major components of balance of payments?

10. What is devaluation? **(10 x 3 = 30 marks)**

## PART B

**(Answer one full question from each module, each question carries 14 marks)**

### MODULE I

11. a) Prepare a utility schedule showing units of consumption, total utility and marginal utility, and explain the law of diminishing marginal utility. Point out any three limitations of the law.

b) How is elasticity of demand measured according to the percentage method? How is the measurement of elasticity of demand useful for the government?

**Or**

12. a) Explain the concepts consumer surplus and producer surplus.

b) Suppose the government imposes a tax on a commodity where the tax burden met by the consumers. Draw a diagram and explain dead weight loss. Mark consumer surplus, producer surplus, tax revenue and dead weight loss in the diagram.

### MODULE II

13. a) What are the advantages of large-scale production?

b) Explain Producer equilibrium with the help of isoquants and isocost line. What is expansion path?

**Or**

14. a) Explain break-even analysis with the help of a diagram.

b) Suppose the monthly fixed cost of a firm is Rs. 40000 and its monthly total variable cost is Rs. 60000.

i. If the monthly sales is Rs. 120000 estimate contribution and break-even sales.

ii. If the firm wants to get a monthly profit of Rs.40000, what should be the sales?

c) The total cost function of a firm is given as $TC=100+50Q - 11Q^2+Q^3$. Find marginal cost when output equals 5 units.

### MODULE III

15. a) What are the features of monopolistic competition?

b) Explain the equilibrium of a firm earning supernormal profit under monopolistic competition.

**Or**

16. a) Make comparison between perfect competition and monopoly.

b) Explain price rigidity under oligopoly with the help of a kinked demand curve.

**MODULE IV**

17. a) How is national income estimated under product method and expenditure method?

b) Estimate GDPmp, GNPmp and National income

| | |
|---|---|
| Private consumption expenditure | = 2000 (in 000 cores) |
| Government Consumption | = 500 |
| NFIA | = -(300) |
| Investment | = 800 |
| Net=exports | =700 |
| Depreciation | = 400 |
| Net-indirect tax | = 300 |

**Or**

18. a) What are the monetary and fiscal policy measures to control inflation?

b) What is SENSEX?

**MODULE V**

19. a) What are the advantages of disadvantages of foreign trade?

b) Explain the comparative cost advantage.

**Or**

20. a) What are the arguments in favour protection?

b) Examine the tariff and non-tariff barriers to international trade.

**(5 × 14 = 70 marks)**

**Teaching Plan**

| | | |
|---|---|---|
| **Module 1 (Basic concepts and Demand and Supply Analysis)** | | **7 Hours** |
| 1.1 | Scarcity and choice – Basic economic problems - PPC | 1 Hour |
| 1.2 | Firms and its objectives – types of firms | 1 Hour |
| 1.3 | Utility – Law of diminishing marginal utility – Demand – law of demand | 1 Hour |
| 1.4 | Measurement of elasticity and its applications | 1 Hour |
| 1.5 | Supply, law of supply and determinants of supply | 1 Hour |
| 1.6 | Equilibrium – changes in demand and supply and its effects | 1 Hour |
| 1.7 | Consumer surplus and producer surplus (Concepts) – Taxation and deadweight loss. | 1 Hour |
| **Module 2 (Production and cost)** | | **7 Hours** |
| 2.1 | Productions function – law of variable proportion | 1 Hour |
| 2.2 | Economies of scale – internal and external economies | 1 Hour |
| 2.3 | producers equilibrium – Expansion path | 1 Hour |
| 2.4 | Technical progress and its implications – cob Douglas Production function | 1 Hour |
| 2.5 | Cost concepts – social cost: private cost and external cost – Explicit and implicit cost – sunk cost | 1 Hour |
| 2.6 | Short run cost curves & Long run cost curves | 1 Hour |
| 2.7 | Revenue (concepts) – shutdown point – Break-even point. | 1 Hour |
| **Module 3 (Market Structure)** | | **6 hours** |
| 3.1 | Equilibrium of a firm, MC – MR approach and TC – TR approach | 1 Hour |
| 3.2 | Perfect competition & Imperfect competition | 1 Hour |
| 3.3 | Monopoly – Regulation of monopoly – Monopolistic competition | 1 Hour |
| 3.4 | Oligopoly – kinked demand curve | 1 Hour |
| 3.5 | Collusive oligopoly (meaning) – Non price competition | 1 Hour |
| 3.6 | Cost plus pricing – Target return pricing – Penetration, Predatory pricing – Going rate pricing – price skimming | 1 Hour |

| | | |
|---|---|---|
| **Module 4 (Macroeconomic concepts)** | | **7 Hours** |
| 4.1 | Circular flow of economic activities | 1 Hour |
| 4.2 | Stock and flow – Final goods and intermediate goods – Gross Domestic Product - National income – Three sectors of an economy | 1 Hour |
| 4.3 | Methods of measuring national income | 1 Hour |
| 4.4 | Inflation – Demand pull and cost push – Causes and effects | 1 Hour |
| 4.5 | Measures to control inflation – Monetary and fiscal policies | 1 Hour |
| 4.6 | Business financing – Bonds and shares – Money market and capital market | 1 Hour |
| 4.7 | Stock market – Demat account and Trading account – SENSEX and NIFTY | 1 Hour |
| **Module 5 (International Trade)** | | **8 Hours** |
| 5.1 | Advantages and disadvantages of international trade | 1 Hour |
| 5.2 | Absolute and comparative advantage theory | 2 Hour |
| 5.3 | Heckscher – Ohlin theory | 1 Hour |
| 5.4 | Balance of payments - components | 1 Hour |
| 5.5 | Balance of payments deficit and devaluation | 1 Hour |
| 5.6 | Trade policy – Free trade versus protection | 1 Hour |
| 5.7 | Tariff and non tariff barriers. | 1 Hour |

| HUT 310 | Management for Engineers | Category | L | T | P | Credit |
|---|---|---|---|---|---|---|
| | | HMC | 3 | 0 | 0 | 3 |

**Preamble**: This course is intended to help the students to learn the basic concepts and functions of management and its role in the performance of an organization and to understand various decision-making approaches available for managers to achieve excellence. Learners shall have a broad view of different functional areas of management like operations, human resource, finance and marketing.

**Prerequisite**: Nil

**Course Outcomes** After the completion of the course the student will be able to

| | |
|---|---|
| **CO1** | Explain the characteristics of management in the contemporary context (Cognitive Knowledge level: **Understand**). |
| **CO2** | Describe the functions of management (Cognitive Knowledge level: **Understand**). |
| **CO3** | Demonstrate ability in decision making process and productivity analysis (Cognitive Knowledge level: **Understand**). |
| **CO4** | Illustrate project management technique and develop a project schedule (Cognitive Knowledge level: **Apply**). |
| **CO5** | Summarize the functional areas of management (Cognitive Knowledge level: **Understand**). |
| **CO6** | Comprehend the concept of entrepreneurship and create business plans (Cognitive Knowledge level: **Understand**). |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | **2** | | | | **1** | **2** | **2** | **2** | | **2** | **1** | **1** |
| **CO2** | **2** | | | | **1** | **1** | | **2** | **1** | **2** | **1** | **1** |
| **CO3** | **2** | **2** | **2** | **2** | **1** | | | | | | | |
| **CO4** | **2** | **2** | **2** | **2** | **1** | | | | | | **2** | **1** |
| **CO5** | **2** | | | | | **1** | **1** | | **1** | **2** | **1** | |
| **CO6** | | **2** | **2** | **2** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

| **Abstract POs defined by National Board of Accreditation** | | | |
|---|---|---|---|
| PO1 | Engineering Knowledge | PO7 | Environment and Sustainability |
| PO2 | Problem Analysis | PO8 | Ethics |
| PO3 | Design/Development of solutions | PO9 | Individual and team work |
| PO4 | Conduct investigations of complex problems | PO10 | Communication |
| PO5 | Modern tool usage | PO11 | Project Management and Finance |
| PO6 | The Engineer and Society | PO12 | Life long learning |

**Assessment Pattern**

| **Bloom's Category** | **Test 1 (Marks in percentage)** | **Test 2 (Marks in percentage)** | **End Semester Examination (Marks in percentage)** |
|---|---|---|---|
| Remember | 15 | 15 | 30 |
| Understand | 15 | 15 | 30 |
| Apply | 20 | 20 | 40 |
| Analyse | | | |
| Evaluate | | | |
| Create | | | |

**Mark Distribution**

| Total Marks | CIE Marks | ESE Marks | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 Hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks

Continuous Assessment - Test : 25 marks

Continuous Assessment - Assignment : 15 marks

**Internal Examination Pattern:**

Each of the two internal examinations has to be conducted out of 50 marks. First series test shall be preferably conducted after completing the first half of the syllabus and the second series test shall be preferably conducted after completing remaining part of the syllabus. There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly completed module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly completed module), each with 7 marks. Out of the 7 questions, a student should answer any 5.

**End Semester Examination Pattern:**

There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

## SYLLABUS

### HUT 310 Management for Engineers (35 hrs)

### Module 1 (Introduction to management Theory- 7 Hours)

Introduction to management theory, Management Defined, Characteristic of Management, Management as an art-profession, System approaches to Management, Task and Responsibilities of a professional Manager, Levels of Manager and Skill required.

### Module 2 (management and organization- 5 hours)

Management Process, Planning types , Mission, Goals, Strategy, Programmes, Procedures, Organising, Principles of Organisation, Delegation, Span of Control, Organisation Structures, Directing, Leadership, Motivation, Controlling..

### Module 3 (productivity and decision making- 7 hours)

Concept of productivity and its measurement; Competitiveness; Decision making process; decision making under certainty, risk and uncertainty; Decision trees; Models of decision making.

### . Module 4 (project management- 8 hours)

Project Management, Network construction, Arrow diagram, Redundancy. CPM and PERT Networks, Scheduling computations, PERT time estimates, Probability of completion of project, Introduction to crashing.

### Module 5 (functional areas of management- 8 hours)

Introduction to functional areas of management, Operations management, Human resources management, Marketing management, Financial management, Entrepreneurship, Business plans, Corporate social responsibility, Patents and Intellectual property rights.

**References:**

1. H. Koontz, and H. Weihrich, Essentials of Management: An International Perspective. 8th ed., McGraw-Hill, 2009.
2. P C Tripathi and P N Reddy, Principles of management, TMH, 4th edition, 2008.
3. P. Kotler, K. L. Keller, A. Koshy, and M. Jha, Marketing Management: A South Asian Perspective. 14th ed., Pearson, 2012.
4. M. Y. Khan, and P. K. Jain, Financial Management, Tata-McGraw Hill, 2008.
5. R. D. Hisrich, and M. P. Peters, Entrepreneurship: Strategy, Developing, and Managing a New Enterprise, 4th ed., McGraw-Hill Education, 1997.
6. D. J. Sumanth, Productivity Engineering and Management, McGraw-Hill Education, 1985.
7. K.Ashwathappa, 'Human Resources and Personnel Management', TMH, 3 rd edition, 2005.
8. R. B. Chase, Ravi Shankar and F. R. Jacobs, Operations and Supply Chain Management, 14th ed. McGraw Hill Education (India), 2015.

**Sample Course Level Assessment Questions**

**Course Outcome1 (CO1):** Explain the systems approach to management?

**Course Outcome 2 (CO2):** Explain the following terms with a suitable example Goal, Objective, and Strategy.

**Course Outcome 3 (CO3):** Mr. Shyam is the author of what promises to be a successful novel. He has the option to either publish the novel himself or through a publisher. The publisher is offering Mr. Shyam Rs. 20,000 for signing the contract. If the novel is successful, it will sell 200,000 copies. Else, it will sell 10,000 copies only. The publisher pays a Re. 1 royalty per copy. A market survey indicates that there is a 70% chance that the novel will be successful. If Mr. Shyam undertakes publishing, he will incur an initial cost of Rs. 90,000 for printing and marketing., but each copy sold will net him Rs. 2. Based on the given information and the

decision analysis method, determine whether Mr. Shyam should accept the publisher's offer or publish the novel himself.

**Course Outcome 4 (CO4):** Explain the concepts of crashing and dummy activity in project management.

**Course Outcome 5 (CO5):** Derive the expression for the Economic order quantity (EOQ)?

**Course Outcome 6 (CO6):** Briefly explain the theories of Entrepreneurial motivation.?

**Model Question Paper**

QP CODE: PAGES: 4

Reg No:_____ Name:_____

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

**FOURTH SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR**

**Course Code: HUT 310**

**Course name: Management for Engineers**

**Max Marks: 100** **Duration: 3 Hours**

**PART-A (Answer All Questions. Each question carries 3 marks)**

1. "Management is getting things done through other." Elaborate.

2. Comment on the true nature of management. Is it a science or an art?

3. Planning is looking ahead and controlling is looking back. Comment with suitable examples

4. Explain the process of communication?

5. Explain the hierarchy of objectives?

6. Explain the types of decisions?

7. Describe the Economic man model?

8. Explain the concepts of crashing and dummy activity in project management.

9. Differentiate the quantitative and qualitative methods in forecasting.

10. What are the key metrics for sustainability measurement? What makes the measurement and reporting of sustainability challenging?

**PART-B (Answer any one question from each module)**

11. a) Explain the systems approach to management. **(10)**

b) Describe the roles of a manager **(4)**

**OR**

12. a) Explain the 14 principles of administrative management? **(10)**

b) Explain the different managerial skills **(4)**

13. a) What are planning premises, explain the classification of planning premises. **(10)**

b) Distinguish between strategy and policy. How can policies be made effective. **(4)**

**OR**

14 a) Explain three motivational theories. **(9)**

b) Describe the managerial grid. **(5)**

15. a) Modern forest management uses controlled fires to reduce fire hazards and to stimulate new forest growth. Management has the option to postpone or plan a burning. In a specific forest tract, if burning is postponed, a general administrative cost of Rs. 300 is incurred. If a controlled burning is planned, there is a 50% chance that good weather will prevail and burning will cost Rs. 3200. The results of the burning may be either successful with probability 0.6 or marginal with probability 0.4. Successful execution will result in an estimated benefit of Rs. 6000, and marginal execution will provide only Rs. 3000 in benefits. If the weather is poor, burning will be cancelled incurring a cost of Rs. 1200 and no benefit. i) Develop a decision tree for the problem. (ii) Analyse the decision tree and determine the optimal course of action. **(8)**

**b)** Student tuition at ABC University is $100 per semester credit hour. The Education department supplements the university revenue by matching student tuition, dollars per dollars. Average class size for typical three credit course is 50 students. Labour costs are $4000 per class, material costs are $20 per student, and overhead cost are $25,000 per class. (a) Determine the total factor productivity. (b) If instructors deliver lecture 14 hours per week and the semester lasts for 16 weeks, what is the labour productivity? **(6)**

**OR**

16. a) An ice-cream retailer buys ice cream at a cost of Rs. 13 per cup and sells it for Rs. 20 per cup; any remaining unsold at the end of the day, can be disposed at a salvage price of Rs. 2.5 per cup. Past sales have ranged between 13 and 17 cups per day; there is no reason to believe that

sales volume will take on any other magnitude in future. Find the expected monetary value and EOL, if the sales history has the following probabilities: **(9)**

| **Market Size** | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|
| **Probability** | 0.10 | 0.15 | 0.15 | 0.25 | 0.35 |

b) At Modem Lumber Company, Kishore the president and a producer of an apple crates sold to growers, has been able, with his current equipment, to produce 240 crates per 100 logs. He currently purchases 100 logs per day, and each log required 3 labour hours to process. He believes that he can hire a professional buyer who can buy a better quality log at the same cost. If this is the case, he increases his production to 260 crates per 100 logs. His labour hours will increase by 8 hours per day. What will be the impact on productivity (measured in crates per labour-hour) if the buyer is hired? What is the growth in productivity in this case? **(5)**

17. a) A project has the following list of activities and time estimates:

| **Activity** | **Time (Days)** | **Immediate Predecessors** |
|---|---|---|
| A | 1 | - |
| B | 4 | A |
| C | 3 | A |
| D | 7 | A |
| E | 6 | B |
| F | 2 | C, D |
| G | 7 | E, F |
| H | 9 | D |
| I | 4 | G, H |

**(a)** Draw the network. (b) Show the early start and early finish times. (c) Show the critical path. **(10)**

b) An opinion survey involves designing and printing questionnaires, hiring and training personnel, selecting participants, mailing questionnaires and analysing data. Develop the precedence relationships and construct the project network. **(4)**

**OR**

18. a) The following table shows the precedence requirements, normal and crash times, and normal and crash costs for a construction project:

| Activity | Immediate Predecessors | Required Time (Weeks) | | Cost (Rs.) | |
|---|---|---|---|---|---|
| | | Normal | Crash | Normal | Crash |
| A | - | 4 | 2 | 10,000 | 11,000 |
| B | A | 3 | 2 | 6,000 | 9,000 |
| C | A | 2 | 1 | 4,000 | 6,000 |
| D | B | 5 | 3 | 14,000 | 18,000 |
| E | B, C | 1 | 1 | 9,000 | 9,000 |
| F | C | 3 | 2 | 7,000 | 8,000 |
| G | E, F | 4 | 2 | 13,000 | 25,000 |
| H | D, E | 4 | 1 | 11,000 | 18,000 |
| I | H, G | 6 | 5 | 20,000 | 29,000 |

Draw the network. (b) Determine the critical path. (c) Determine the optimal duration and the associated cost. **(10)**

b) Differentiate between CPM and PERT. **(4)**

19. a) What is meant by market segmentation and explain the process of market segmentation **(8)**

b) The Honda Co. in India has a division that manufactures two-wheel motorcycles. Its budgeted sales for Model G in 2019 are 80,00,000 units. Honda's target ending inventory is 10,00, 000 units and its beginning inventory is 12, 00, 000 units. The company's budgeted selling price to its distributors and dealers is Rs. 40, 000 per motorcycle. Honda procures all its wheels from an

outside supplier. No defective wheels are accepted. Honda's needs for extra wheels for replacement parts are ordered by a separate division of the company. The company's target ending inventory is 3,00,000 wheels and its beginning inventory is 2,00,000 wheels. The budgeted purchase price is Rs. 1,600 per wheel.

(a) Compute the budgeted revenue in rupees.

(b) Compute the number of motorcycles to be produced.

Compute the budgeted purchases of wheels in units and in rupees.? **(6)**

**OR**

20. a) a) "Human Resource Management policies and principles contribute to effectiveness, continuity and stability of the organization". Discuss. (b) What is a budget? Explain how sales budget and production budgets are prepared? **(10)**

b) Distinguish between the following: (a) Assets and Liabilities (b) Production concept and Marketing concept (c) Needs and Wants (d) Design functions and Operational control functions in operations **(4)**

**Teaching Plan**

| Sl.No | TOPIC | SESSION |
|---|---|---|
| | **Module I** | |
| 1.1 | Introduction to management | 1 |
| 1.2 | Levels of managers and skill required | 2 |
| 1.3 | Classical management theories | 3 |
| 1.4 | neo-classical management theories | 4 |
| 1.5 | modern management theories | 5 |
| 1.6 | System approaches to Management, | 6 |
| 1.7 | Task and Responsibilities of a professional Manager | 7 |
| | **Module 2** | |
| 2.1 | Management process – planning | 8 |
| 2.2 | Mission – objectives – goals – strategy – policies – programmes – procedures | 9 |
| 2.3 | Organizing, principles of organizing, organization structures | 10 |
| 2.4 | Directing, Leadership | 11 |
| 2.5 | Motivation, Controlling | 12 |
| | **Module III** | |
| 3.1 | Concept of productivity and its measurement Competitiveness | 13 |
| 3.2 | Decision making process; | 14 |
| 3.3 | Models in decision making | 15 |
| 3.4 | Decision making under certainty and risk | 16 |
| 3.5 | Decision making under uncertainty | 17 |
| 3.6 | Decision trees | 18 |
| 3.7 | Models of decision making. | 19 |
| | **Module IV** | |
| 4.1 | Project Management | 20 |

| Sl.No | TOPIC | SESSION |
|---|---|---|
| | **Module I** | |
| 4.2 | Network construction | 21 |
| 4.3 | Arrow diagram, Redundancy | 22 |
| 4.4 | CPM and PERT Networks | 23 |
| 4.5 | Scheduling computations | 24 |
| 4.6 | PERT time estimates | 25 |
| 4.7 | Probability of completion of project | 26 |
| 4.8 | Introduction to crashing | |
| | **Module V** | |
| 5.1 | Introduction to functional areas of management, | 28 |
| 5.2 | Operations management | 29 |
| 5.3 | Human resources management , | 30 |
| 5.4 | Marketing management | 31 |
| 5.5 | Financial management | 32 |
| 5.6 | Entrepreneurship, | 33 |
| 5.7 | Business plans | 34 |
| 5.8 | Corporate social responsibility, Patents and Intellectual property rights | 35 |

| MCN 301 | DISASTER MANAGEMENT | Category | L | T | P | CREDIT | YEAR OF INTRODUCTION |
|---|---|---|---|---|---|---|---|
| | | Non - Credit | 2 | 0 | 0 | Nil | 2019 |

**Preamble**: The objective of this course is to introduce the fundamental concepts of hazards and disaster management.

**Prerequisite**: Nil

**Course Outcomes**: After the completion of the course the student will be able to

| | |
|---|---|
| **CO1** | Define and use various terminologies in use in disaster management parlance and organise each of these terms in relation to the disaster management cycle (Cognitive knowledge level: **Understand**). |
| **CO2** | Distinguish between different hazard types and vulnerability types and do vulnerability assessment (Cognitive knowledge level: **Understand**). |
| **CO3** | Identify the components and describe the process of risk assessment, and apply appropriate methodologies to assess risk (Cognitive knowledge level: **Understand**). |
| **CO4** | Explain the core elements and phases of Disaster Risk Management and develop possible measures to reduce disaster risks across sector and community (Cognitive knowledge level: **Apply**) |
| **CO5** | Identify factors that determine the nature of disaster response and discuss the various disaster response actions (Cognitive knowledge level: **Understand**). |
| **CO6** | Explain the various legislations and best practices for disaster management and risk reduction at national and international level (Cognitive knowledge level: **Understand**). |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO 9 | PO1 0 | PO1 1 | PO1 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | | 2 | | | | 2 | | | | 2 | | 2 |
| **CO2** | 2 | 3 | 2 | | 2 | 2 | 3 | | | 3 | | 2 |
| **CO3** | 2 | 3 | 2 | 2 | 2 | 2 | 3 | | | 3 | | 2 |
| **CO4** | 3 | 3 | 3 | | 2 | 2 | 3 | | | | | 2 |
| **CO5** | 3 | 3 | | | 2 | 2 | 3 | | | | | 2 |
| **CO6** | 3 | | | | | 2 | 3 | 3 | | | | 2 |

| **Abstract POs defined by National Board of Accreditation** | | | |
|---|---|---|---|
| **PO#** | **Broad PO** | **PO#** | **Broad PO** |
| PO1 | Engineering Knowledge | PO7 | Environment and Sustainability |
| PO2 | Problem Analysis | PO8 | Ethics |
| PO3 | Design/Development of solutions | PO9 | Individual and team work |
| PO4 | Conduct investigations of complex problems | PO10 | Communication |
| PO5 | Modern tool usage | PO11 | Project Management and Finance |
| PO6 | The Engineer and Society | PO12 | Life long learning |

**Assessment Pattern**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination Marks |
|---|---|---|---|
| | Test 1 (Marks) | Test 2 (Marks) | |
| Remember | **10** | **10** | **20** |
| Understand | **25** | **25** | **50** |
| Apply | **15** | **15** | **30** |
| Analyze | | | |
| Evaluate | | | |
| Create | | | |

**Mark Distribution**

| Total Marks | CIE Marks | ESE Marks | ESE Duration |
|---|---|---|---|
| **150** | **50** | **100** | **3 hours** |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks

Continuous Assessment - Test : 25 marks

Continuous Assessment - Assignment : 15 marks

**Internal Examination Pattern:**

Each of the two internal examinations has to be conducted out of 50 marks. First series test shall be preferably conducted after completing the first half of the syllabus and the second series test shall be preferably conducted after completing remaining part of the syllabus. There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly completed module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A.

Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly completed module), each with 7 marks. Out of the 7 questions, a student should answer any 5.

**End Semester Examination Pattern:**

There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

## SYLLABUS

## MCN 301 Disaster Management

**Module 1**

Systems of earth

Lithosphere- composition, rocks, soils; Atmosphere-layers, ozone layer, greenhouse effect, weather, cyclones, atmospheric circulations, Indian Monsoon; hydrosphere- Oceans, inland water bodies; biosphere

Definition and meaning of key terms in Disaster Risk Reduction and Management- disaster, hazard, exposure, vulnerability, risk, risk assessment, risk mapping, capacity, resilience, disaster risk reduction, disaster risk management, early warning systems, disaster preparedness, disaster prevention, disaster mitigation, disaster response, damage assessment, crisis counselling, needs assessment.

**Module 2**

Hazard types and hazard mapping; Vulnerability types and their assessment- physical, social, economic and environmental vulnerability.

Disaster risk assessment –approaches, procedures

**Module 3**

Disaster risk management -Core elements and phases of Disaster Risk Management

Measures for Disaster Risk Reduction – prevention, mitigation, and preparedness.

Disaster response- objectives, requirements; response planning; types of responses.

Relief; international relief organizations.

**Module 4**

Participatory stakeholder engagement; Disaster communication- importance, methods, barriers; Crisis counselling

Capacity Building: Concept – Structural and Non-structural Measures, Capacity Assessment; Strengthening Capacity for Reducing Risk

**Module 5**

Common disaster types in India; Legislations in India on disaster management; National disaster management policy; Institutional arrangements for disaster management in India.

The Sendai Framework for Disaster Risk Reduction- targets, priorities for action, guiding principles

**Reference Text Book**


1. R. Subramanian, Disaster Management, Vikas Publishing House, 2018
2. M. M. Sulphey, Disaster Management, PHI Learning, 2016
3. UNDP, Disaster Risk Management Training Manual, 2016
4. United Nations Office for Disaster Risk Reduction, Sendai Framework for Disaster Risk Reduction 2015-2030, 2015


**Sample Course Level Assessment Questions**

**Course Outcome 1 (CO1):**

1. What is the mechanism by which stratospheric ozone protects earth from harmful UV rays?
2. What are disasters? What are their causes?
3. Explain the different types of cyclones and the mechanism of their formation
4. Explain with examples, the difference between hazard and risk in the context of disaster management
5. Explain the following terms in the context of disaster management (a) exposure (b) resilience (c) disaster risk management (d) early warning systems, (e) damage assessment (f) crisis counselling (g) needs assessment

**Course Outcome 2 (CO2):**

1. What is hazard mapping? What are its objectives?
2. What is participatory hazard mapping? How is it conducted? What are its advantages?
3. Explain the applications of hazard maps
4. Explain the types of vulnerabilities and the approaches to assess them

**Course Outcome 3 (CO3):**

1. Explain briefly the concept of ‘disaster risk’

2. List the strategies for disaster risk management 'before', 'during' and 'after' a disaster
3. What is disaster preparedness? Explain the components of a comprehensive disaster preparedness strategy

**Course Outcome 4 (CO4):**

1. What is disaster prevention? Distinguish it from disaster mitigation giving examples
2. What are the steps to effective disaster communication? What are the barriers to communication?
3. Explain capacity building in the context of disaster management

**Course Outcome 5 (CO5):**

1. Briefly explain the levels of stakeholder participation in the context of disaster risk reduction
2. Explain the importance of communication in disaster management
3. Explain the benefits and costs of stakeholder participation in disaster management
4. How are stakeholders in disaster management identified?

**Course Outcome 6 (CO6):**

1. Explain the salient features of the National Policy on Disaster Management in India
2. Explain the guiding principles and priorities of action according to the Sendai Framework for Disaster Risk Reduction
3. What are Tsunamis? How are they caused?
4. Explain the earthquake zonation of India

**Model Question paper**

**QP CODE:** **PAGES:3**

**Reg No:_____** **Name :_____**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

**FIFTH SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR**

**Course Code: MCN 301**

**Course Name: Disaster Management**

**Max.Marks:100** **Duration: 3 Hours**

**PART A**

**Answer all Questions. Each question carries 3 Marks**

1. What is the mechanism by which stratospheric ozone protects earth from harmful UV rays?
2. What are disasters? What are their causes?
3. What is hazard mapping? What are its objectives?
4. Explain briefly the concept of 'disaster risk'
5. List the strategies for disaster risk management 'before', 'during' and 'after' a disaster
6. What is disaster prevention? Distinguish it from disaster mitigation giving examples
7. Briefly explain the levels of stakeholder participation in the context of disaster risk reduction
8. Explain the importance of communication in disaster management
9. What are Tsunamis? How are they caused?
10. Explain the earthquake zonation of India

**Part B**

**Answer any one Question from each module. Each question carries 14 Marks**

11. a. Explain the different types of cyclones and the mechanism of their formation [10]

b. Explain with examples, the difference between hazard and risk in the context of disaster management
[4]

OR

12. Explain the following terms in the context of disaster management [14]

(a) exposure (b) resilience (c) disaster risk management (d) early warning systems, (e) damage assessment (f) crisis counselling (g) needs assessment

13. a. What is participatory hazard mapping? How is it conducted? What are its advantages?

[8]

b. Explain the applications of hazard maps [6]

OR

14. Explain the types of vulnerabilities and the approaches to assess them [14]

15. a. Explain the core elements of disaster risk management [8]

b. Explain the factors that decide the nature of disaster response [6]

OR

16. a. What is disaster preparedness? Explain the components of a comprehensive disaster preparedness strategy [6]

b. Explain the different disaster response actions [8]

17. a. Explain the benefits and costs of stakeholder participation in disaster management [10]

b. How are stakeholders in disaster management identified? [4]

OR

18. a. What are the steps to effective disaster communication? What are the barriers to communication? [7]

b. Explain capacity building in the context of disaster management [7]

19. Explain the salient features of the National Policy on Disaster Management in India [14]

OR

20. Explain the guiding principles and priorities of action according to the Sendai Framework for Disaster Risk Reduction [14]

## Teaching Plan

| | Module 1 | 5 Hours |
|---|---|---|
| 1.1 | Introduction about various Systems of earth, Lithosphere-composition, rocks, Soils; Atmosphere-layers, ozone layer, greenhouse effect, weather | 1 Hour |
| 1.2 | Cyclones, atmospheric circulations, Indian Monsoon; hydrosphere-Oceans, inland water bodies; biosphere | 1 Hour |
| 1.3 | Definition and meaning of key terms in Disaster Risk Reduction and Management- disaster, hazard, | 1 Hour |
| 1.4 | Exposure, vulnerability, risk, risk assessment, risk mapping, capacity, resilience, disaster risk reduction, Disaster risk management, early warning systems | 1 Hour |
| 1.5 | Disaster preparedness, disaster prevention, disaster, Mitigation, disaster response, damage assessment, crisis counselling, needs assessment. | 1 Hour |
| | **Module 2** | **5 Hours** |
| 2.1 | Various Hazard types, Hazard mapping; Different types of Vulnerability types and their assessment | 1 Hour |
| 2.2 | Vulnerability assessment and types, Physical and social vulnerability | 1 Hour |
| 2.3 | Economic and environmental vulnerability, Core elements of disaster risk assessment | 1 Hour |
| 2.4 | Components of a comprehensive disaster preparedness strategy approaches, procedures | 1 Hour |
| 2.5 | Different disaster response actions | 1 Hour |
| | **Module 3** | **5 Hours** |
| 3.1 | Introduction to Disaster risk management, Core elements of Disaster Risk Management | 1 Hour |
| 3.2 | Phases of Disaster Risk Management, Measures for Disaster Risk Reduction | 1 Hour |
| 3.3 | Measures for Disaster prevention, mitigation, and preparedness. | 1 Hour |

| | | |
|---|---|---|
| 3.4 | Disaster response- objectives, requirements. Disaster response planning; types of responses. | 1 Hour |
| 3.5 | Introduction- Disaster Relief, Relief; international relief organizations. | 1 Hour |
| | **Module 4** | **5 Hours** |
| 4.1 | Participatory stakeholder engagement | 1 Hour |
| 4.2 | Importance of disaster communication. | 1 Hour |
| 4.3 | Disaster communication- methods, barriers. Crisis counselling | 1 Hour |
| 4.4 | Introduction to Capacity Building. Concept – Structural Measures, Non-structural Measures. | 1 Hour |
| 4.5 | Introduction to Capacity Assessment, Capacity Assessment; Strengthening, Capacity for Reducing Risk | 1 Hour |
| | **Module 5** | **5 Hours** |
| 5.1 | Introduction-Common disaster types in India. | 1 Hour |
| 5.2 | Common disaster legislations in India on disaster management | 1 Hour |
| 5.3 | National disaster management policy, Institutional arrangements for disaster management in India. | 1 Hour |
| 5.4 | The Sendai Framework for Disaster Risk Reduction and targets | 1 Hour |
| 5.5 | The Sendai Framework for Disaster Risk Reduction-priorities for action, guiding principles | 1 Hour |

| ECL331 | ANALOG INTEGRATED CIRCUITS AND SIMULATION LAB | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 0 | 0 | 3 | 2 |

**Preamble:** This course aims to (i) familiarize students with the Analog Integrated Circuits and Design and implementation of application circuits using basic Analog Integrated Circuits (ii) familiarize students with simulation of basic Analog Integrated Circuits.

**Prerequisite:** ECL202 Analog Circuits and Simulation Lab

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO 1** | Use data sheets of basic Analog Integrated Circuits and design and implement application circuits using Analog ICs. |
| **CO 2** | Design and simulate the application circuits with Analog Integrated Circuits using simulation tools. |
| **CO 3** | Function effectively as an individual and in a team to accomplish the given task. |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO 2 | PO3 | PO 4 | PO5 | PO 6 | PO7 | PO8 | PO9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | | | | | | 2 | | | 2 |
| **CO2** | 3 | 3 | 3 | 2 | 3 | | | | 2 | | | 2 |
| **CO3** | 2 | 2 | 2 | | 2 | | | | 3 | 2 | | 3 |

**Assessment**
**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 75 | 75 | 3 hours |

**Continuous Evaluation Pattern**

Attendance : 15 marks
Continuous Assessment : 30 marks
Internal Test (Immediately before the second series test) : 30 marks

**End Semester Examination Pattern:** The following guidelines should be followed regarding awardof marks

(a) Preliminary work : 15 Marks

(b) Implementing the work/Conducting the experiment : 10 Marks

(c) Performance, result and inference (usage of equipments and trouble shooting): 25 Marks

(d) Viva voce : 20 marks

(e) Record : 5 Marks

**General instructions:** End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

**Course Level Assessment Questions (Examples only)**

**Course Outcome 1 (CO1):** Use data sheets of basic Analog Integrated Circuits and design and implement application circuits using Analog ICs.

1. Measure important opamp parameters of µA 741 and compare them with the data provided in the data sheet
2. Design and implement a variable timer circuit using opamp
3. Design and implement a filter circuit to eliminate 50 Hz power line noise.

**Course Outcome 2 and 3 (CO2 and CO3):** Design and simulate the application circuits with Analog Integrated Circuits using simulation tools.

1. Design a precission rectifier circuit using opamps and simulste it using SPICE
2. Design and simulate a counter ramp ADC

**List of Experiments**

**I.** Fundamentals of operational amplifiers and basic circuits [Minimum seven experiments are to be done]

1. Familiarization of Operational amplifiers - Inverting and Non inverting amplifiers, frequency response, Adder, Integrator, Comparators.
2. Measurement of Op-Amp parameters.
3. Difference Amplifier and Instrumentation amplifier.
4. Schmitt trigger circuit using Op–Amps.
5. Astable and Monostable multivibrator using Op-Amps.
6. Waveform generators using Op-Amps - Triangular and saw tooth
7. Wien bridge oscillator using Op-Amp - without & with amplitude stabilization.

8. RC Phase shift Oscillator.
9. Active second order filters using Op-Amp (LPF, HPF, BPF and BSF).
10. Notch filters to eliminate the 50Hz power line frequency.
11. Precision rectifiers using Op-Amp.

**II.** Application circuits of **555 Timer/565 PLL/ Regulator(IC 723) ICs** [ Minimum three experiments are to be done]

1. Astable and Monostable multivibrator using Timer IC NE555
2. DC power supply using IC 723: Low voltage and high voltage configurations, Short circuit and Fold-back protection.
3. A/D converters- counter ramp and flash type.
4. D/A Converters - R-2R ladder circuit
5. Study of PLL IC: free running frequency lock range capture range

**III. Simulation experiments [The experiments shall be conducted using SPICE]**

1. Simulation of any three circuits from Experiments 3, 5, 6, 7, 8, 9, 10 and 11 of section I
2. Simulation of Experiments 3 or 4 from section II

**Textbooks**

1. D. Roy Choudhary, Shail B Jain, "Linear Integrated Circuits,"
2. M. H. Rashid, "Introduction to Pspice Using Orcad for Circuits and Electronics", Prentice Hall

| SEMESTER VI ( BTech VLSI Design and Technology) | | | | | | |
|---|---|---|---|---|---|---|
| **SLOT** | **COURSE NO.** | **COURSES** | **L-T-P** | **HOURS** | **CREDIT** | **REMARKS** |
| A | EVT 302 | ANALOG CMOS DESIGN | 3-1-0 | 4 | 4 | NEW SYLLABUS |
| B | EVT 304 | ***SOC DESIGN*** | 3-1-0 | 4 | 4 | ‘’ |
| C | EVT 306 | DIGITAL SIGNAL PROCESSING | 3-1-0 | 4 | 4 | ,, |
| D | E..T XXX | PROGRAM ELECTIVE I | 2-1-0 | 3 | 3 | |
| E ½ | HUT300 | INDUSTRIAL ECONOMICS AND FOREIGN TRADE | 3-0-0 | 3 | 3 | **EXISTING SYLLABUS of EC** |
| | HUT310 | MANAGEMENT FOR ENGINEERS | 3-0-0 | 3 | 3 | ,, |
| F | ECT 308 | COMPREHENSIVE COURSE WORK | 1-0-0 | 1 | 1 | |
| S | EVL 332 | VLSI DESIGN LAB | 0-0-3 | 3 | 2 | NEW SYLLABUS |
| T | ECD 334 | MINI PROJECT | 0-0-3 | 3 | 2 | **EXISTING SYLLABUS of EC** |
| R/M/H | VAC | Remedial/Minor/Honours | 3-1-0 | 4** | 4 | |
| TOTAL | | | | 25/29 | 23/27 | |

PROGRAM ELECTIVE I

| Code | Course Name |
|---|---|
| ECT302 | Electromagnetics |
| ECT305 | Analog and digital communication |
| ECT332 | Data analysis |
| ECT352 | Digital image processing |
| ECT362 | Introduction to MEMS |
| ECT372 | Quantum computing |
| ECT423 | Computer networks |

| EVT302 | ANALOG CMOS DESIGN | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble: This course aim to understand design and working of Analog CMOS Devices**

**Prerequisite:**

**Course Out Comes: A**fter the completion of the course the student will be able to:

| | |
|---|---|
| **CO1** | Design different MOS device models and explain different parameters affecting MOSFET design. |
| **CO2** | Explain the working of differential amplifier and an idea about Gilbert cell and different current mirror techniques. |
| **CO3** | Analyse the frequency response of single-stage and differential amplifiers. |
| **CO4** | Analyse the effect of noise in single-stage amplifiers. |
| **CO5** | Discuss stability analysis of PLL and various applications of PLL. |

**Mapping of course outcomes with program outcomes:**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | | | | | | | | | | 2 |
| **CO2** | 3 | 3 | | | | | | | | | | 2 |
| **CO3** | 3 | 3 | | | | | | | | | | 2 |
| **CO4** | 3 | 3 | | | | | | | | | | 2 |
| **CO5** | 3 | | | | | | | | | | | 2 |

**Assessment Pattern:**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|
| | 1 | 2 | |
| Remember | 10 | 10 | 20 |
| Understand | 20 | 20 | 40 |
| Apply | 10 | 10 | 20 |
| Analyse | 10 | 10 | 20 |
| Evaluate | | | |
| Create | | | |

**Mark distribution:**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 Hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern**

**Maximum Marks: 100** **Time: 3 hours**

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 subdivisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1): Design different MOS device models and explain different parameters affecting MOSFET design.**

1. Analyse MOS with different load types.
2. Explain the terms
   i) Hot carrier effect. ii) Threshold voltage variation. iii) Mobility degradation.
3. Explain different MOS Devices models a) BSIM series b) LEVEL 1,2,3
4. Explain the small-signal model for the MOS Transistor.
5. Design and explain the working of cascode amplifier.

**Course Outcome 2 (CO2): Explain the working of differential amplifier and an idea about Gilbert cell and different current mirror techniques.**

1. Perform Qualitative Analysis of Differential Pair.
2. Examine the operation of differential pair with MOS load.
3. Describe the operation of common mode response in differential amplifier.
4. Design of current mirror circuits.
5. Explain the importance of Gilbert cell.

**Course Outcome 3 (CO3): Analyse the frequency response of single-stage and differential amplifiers.**

1. Calculation of poles associated with the nodes in a circuit.
2. Calculate the voltage transfer function of various MOS configurations
3. Modelling the high frequency equivalent circuit of various configurations.

**Course Outcome 4 (CO4): Analyse the effect of noise in single-stage amplifiers.**

1. Modelling of noise in circuits.

2. Calculation of Input referred noise and output noise in various circuits.

**Course Outcome 5 (CO5): Discuss stability analysis of PLL and various applications of PLL.**

1. Illustrate the operation of PLL
2. Describe the implementation of PLL for Frequency Multiplication, Frequency synthesizer and Skew reduction

**Syllabus**

| Module | Course contents | Hours |
|---|---|---|
| I | Introduction to Analog Design, Review of MOS Characteristics and Second order effects, Scaling Theory, Short- Channel Effects - Threshold Voltage Variation, Mobility Degradation with Vertical Field, Velocity Saturation, Hot Carrier Effects, Output Impedance Variation with Drain-Source Voltage, MOS Device Models - Level 1, Level 2, and Level 3 Models, BSIM Series, Process Corners.<br>Single Stage Amplifiers. Common Source Stage with passive and active load types, Source Follower, Common Gate and Cascode Stage. | 13 |
| II | Differential Amplifiers - Single-ended and differential operation, Basic differential pair, Common-mode response, Differential pair with MOS load, Gilbert Cell.<br>Current Mirror: Simple, Cascode and Basic concepts of Active Current Mirror. | 8 |
| III | Frequency Response of Amplifiers: Miller Effect, Poles and Zeros, Frequency Response Analysis of Common Source, Source Follower, Common Gate and Differential Pair. | 7 |
| IV | Noise in Amplifiers: Statistical Characteristics of Noise, Types of Noise, Representation of Noise in Circuits, Noise in Single-Stage Amplifiers - Common-Source Stage, Common-Gate Stage and Source Follower, Noise-Power Trade-Off, Noise Bandwidth. | 7 |
| V | Phase Locked Loops- Mathematical model of VCO, Phase Detector, Basic PLL Topology, Type I and Type II (Charge Pump) PLL, Stability Analysis of PLL, Non-Ideal Effects in PLL, Application of PLL- Frequency Multiplication, Frequency synthesizer and Skew reduction. Block Diagram of Digital PLL. | 7 |

**Text Books:** 1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2/e, 2002

**References:**


1. Phillip E. Allen, Douglas R. Holbery, CMOS Analog Circuit Design, Oxford, 2004.
2. Razavi B., Fundamentals of Microelectronics, Wiley student Edition 2014.
3. Baker, Li, Boyce, CMOS: Circuits Design, Layout and Simulation, PHI, 2000


**Course Contents and Lecture Schedule.**

| No | Topic | No.of. Lectures |
|---|---|---|
| | **Module I** | |
| 1.1 | Introduction to Analog Design, Review of MOS Characteristics and Second order effects, Scaling Theory | **2** |
| 1.2 | Short- Channel Effects - Threshold Voltage Variation, Mobility Degradation with Vertical Field, Velocity Saturation | **2** |
| 1.3 | Hot Carrier Effects, Output Impedance Variation with Drain-Source Voltage, | **2** |
| 1.4 | MOS Device Models - Level 1, Level 2, and Level 3 Models, BSIM Series, Process Corners. | **2** |
| 1.5 | Single Stage Amplifiers. Common Source Stage with passive and active load types | **2** |
| 1.6 | Source Follower, Common Gate and Cascode Stage. | **1** |
| | TUTORIAL | **2** |
| | **Module II** | |
| 2.1 | Differential Amplifiers - Single-ended and differential operation | **2** |
| 2.2 | Basic differential pair, Common-mode response | **1** |
| 2.3 | Differential pair with MOS load, Gilbert Cell. | **1** |
| 2.4 | Current mirror: Simple, Cascode and basic concepts Active current mirror. | **1** |
| | TUTORIAL | **2** |
| | **Module III** | |
| 3.1 | Frequency Response of Amplifiers: Miller Effect, Poles and Zeros, | **2** |
| 3.2 | Frequency Response Analysis of Common Source Amplifier, | **1** |
| 3.3 | Frequency Response Analysis Source Follower and Common Gate stage | **1** |
| 3.4 | Frequency Response Analysis of Differential amplifier Pair | **1** |
| | TUTORIAL | **2** |
| | **Module IV** | |
| 4.1 | Noise in Amplifiers: Statistical Characteristics of Noise | **1** |
| | Types of Noise, Representation of Noise in Circuits | **1** |

| | | |
|---|---|---|
| 4.2 | | |
| 4.3 | Noise in Single-Stage Amplifiers - Common-Source Stage, Common-Gate Stage and Source Follower | **1** |
| 4.4 | Noise-Power Trade-Off, Noise Bandwidth | **2** |
| | TUTORIAL | **2** |
| **Module V** | | |
| 5.1 | Phase Locked Loops- Mathematical model of VCO | **1** |
| 5.2 | Phase Detector, Basic PLL Topology, Type I and Type II (Charge Pump) PLL | **1** |
| 5.3 | Stability Analysis of PLL, Non-Ideal Effects in PLL | **1** |
| 5.4 | Applications of PLL- Frequency Multiplication, Frequency synthesizer and Skew reduction. Block Diagram of Digital PLL. | **2** |
| | TUTORIAL | **2** |

# Model Question paper

## APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
## SIXTH SEMESTER B. TECH DEGREE EXAMINATION
## Course Code:
## Course Name: ANALOG CMOS DESIGN

Max. Marks:100 Duration: 3 Hours

1 Plot the VI characteristics of NMOS transistor. (3)

2 Explain briefly the working principle of source follower (3)
3 Explain the simplest form of current mirror and bipolar version of the current mirror. (3)
4 What are the limitations of Gilbert Cell. (3)
5 Describe Miller's theorem. (3)
6 Draw and explain the frequency response of common source amplifier (3)
7 Describe the statistical characteristics of noise. (3)
8 Discuss briefly the term Flicker noise. (3)
9 Distinguish between type 1 and type 2 PLL. (3)
10 Why the order of PLL transfer function is lower by one when the PFD operates as frequency detector. (3)

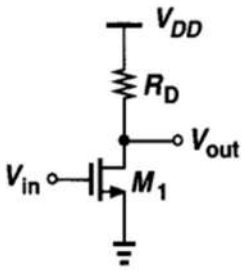
**PART B**
**(Answer one question from each module. Each question carries 14 marks)**

**MODULE I**

11 a) Summarize the Short channel effects in MOS transistors.
b) In the circuit below, assume (W/L)1 = 50/0.5, RD = 2kΩ and λ = 0.

i) What is the small signal gain if M1 is in saturation and ID = 1mA?

ii) What input voltage places M1 at the edge of the triode region? What is the small signal gain under this condition?




OR

12 a) Describe the Level 1 and Level 2 MOS device model.

b) Derive the gain and output impedance of a NMOS transistor with resistive load, draw the circuit diagram and small signal model.

MODULE II

13 a) Design the current mirror shown to provide an output current of I0 = 90μA for 0 ≤ RL ≤15kΩ. Assume the following transistor parameters: L1 = L2 = 1μm, μnCox = 180μA/V2 , Vt = 0.4V, and λ = 0.Use a supply voltage VDD = 1.6V and use minimum values of W1 and W2 for which the current mirror fulfills the specifications. (7)

b) Explain the common mode response of a differential amplifier. (7)

OR

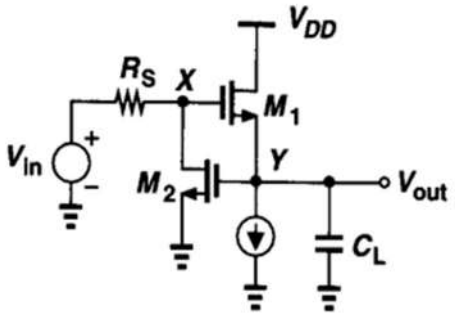
14 a) Explain the operation of a single ended differential amplifier. 7)
b) Define current mirrors? Derive the expression for output current in a current mirror circuit neglecting the channel length modulation. (7)

MODULE III

15 For a common source amplifier, find the input pole, output pole and transfer function. (14)

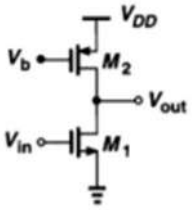
OR

16 Calculate the transfer function of the circuit shown below. (14)




**MODULE IV**

17a) Calculate the total input referred thermal noise voltage of the amplifier shown below. (10)




b) Explain the trade-off between bandwidth and signal to noise ratio in MOS circuits. (4)

OR

18 a) With suitable diagram, explain resistor thermal noise and its spectral density? (7)

b) How can we determine the input – referred noise voltage and current in MOS circuits? (7)

MODULE V

19 a) With a neat diagram, explain the mathematical model of VCO. (8)

b) Describe the causes of stability degradation in charge pump PLL (6)

OR

20 a) Describe various applications of PLL. (10)

b) Explain the operation of a Digital PLL. (4)

| EVT 304 | SOC DESIGN | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:**

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO1** | Differentiate between waterfall and spiral models, and apply top-down and bottom-up design approaches. |
| **CO2** | Create functional and efficient macros based on specified requirements. |
| **CO3** | Recognize different fault models and understand their implications in digital circuit testing. |
| **CO4** | Utilize various BIST methods to generate effective test patterns for fault detection. |
| **CO5** | Verify SoC designs at both system and block levels to ensure overall functionality and performance. |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | | 3 | | | | | | | 2 |
| **CO2** | 3 | 3 | 3 | | 3 | | | | | | | 2 |
| **CO3** | 2 | 2 | 2 | | 2 | | | | | | | 2 |
| **CO4** | 2 | 2 | 2 | | 2 | | | | | | | 2 |
| **CO5** | 2 | 2 | 2 | | 2 | | | | | | | 2 |

**Assessment Pattern**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|
| | 1 | 2 | |

| | | | |
|---|---|---|---|
| Remember K1 | 10 | 10 | 10 |
| Understand K2 | 20 | 20 | 30 |
| Apply K3 | 20 | 20 | 60 |
| Analyse K4 | | | |
| Evaluate | | | |
| Create | | | |

**Mark distribution**

| **Total** | **CIE** | **ESE** | **ESE Duration** |
|---|---|---|---|
| **Marks** | | | |
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1) : Differentiate between waterfall and spiral models, and apply top-down and bottom-up design approaches.**

1. Compare and contrast Soft IP and Hard IP in SoC design.
2. What are the advantages and disadvantages of integrating Soft IP versus Hard IP components?
3. Discuss the challenges associated with integrating Soft IP and Hard IP into a cohesive SoC design.

**Course Outcome 2 (CO2) : Create functional and efficient macros based on specified requirements.**

1. What are the key considerations when defining the top-level design of a macro? How does this initial design phase impact the overall integration and functionality of the macro within a larger system?
2. Describe the process of specifying functional requirements for a macro. How do these requirements guide the design decisions at the top-level?

**Course Outcome 3 (CO3) :**Recognize different fault models and understand their implications in digital circuit testing

1.Define the term "fault" in the context of digital circuits. Provide examples of common faults that can occur in digital circuits.

2. Explain Roth's D-algorithm. How does it generate test patterns to detect faults in digital circuits?

3. Describe the components of an ATPG vector used for testing digital circuits. What information does an ATPG vector contain?

4. Discuss the challenges associated with ensuring comprehensive test coverage in digital circuit testing. How can advanced ATPG techniques address these challenges?

**Course Outcome 4 (CO4) :** Utilize various BIST methods to generate effective test patterns for fault detection.

1. How does the EXTEST instruction differ from the INTEST instruction in boundary scan?
2. What are the components of the Test Access Port (TAP) in boundary scan?
3. Explain how the SAMPLE/PRELOAD instruction is used in boundary scan testing.
4. What is the significance of the BYPASS instruction in boundary scan?
5. What are the advantages of using full integrated scan in testing complex designs?
6. Describe the role of Linear Feedback Shift Registers (LFSRs) in signature analysis.
7. What is the primary purpose of signature analysis in BIST?
8. What are the key components of a Built-In Self-Test (BIST) architecture?
9. How does the Test Pattern Generator (TPG) contribute to BIST?
10. What is the role of the Response Analyzer (RA) in BIST?
11. Explain the advantages of incorporating BIST into a circuit.
12. How does BIST facilitate field testing and diagnostics?
13. What is the difference between exhaustive testing and pseudo-random testing in BIST?
14. How do Linear Feedback Shift Registers (LFSRs) generate pseudo-random test patterns?
15. Describe the function of a counter-based Test Pattern Generator (TPG).
16. What are the benefits of using ROM-based Test Pattern Generators in BIST?
17. Why is deterministic testing important for achieving high fault coverage in BIST?

**Course Outcome 5 (CO5) :** Verify SoC designs at both system and block levels to ensure overall functionality and performance.

1. What are the primary technology options available for SoC verification?
2. How do simulation-based verification technologies compare to emulation-based technologies?
3.What are the advantages and disadvantages of using formal verification in SoC verification?
4.Describe how hardware acceleration can be used in SoC verification.
5. What role do field-programmable gate arrays (FPGAs) play in verification technology?
6. What is the importance of having a verification methodology in SoC design?
7. Describe the Universal Verification Methodology (UVM) and its key components.
8. How does the Coverage-Driven Verification (CDV) methodology enhance SoC verification?
9. What is the role of constrained random verification in modern verification methodologies?
10. Explain the significance of reuse in verification methodology.

## SYLLABUS

| Module | Course contents |
|---|---|
| **I** | System On Chip Design Process: A canonical SoC Design, SoC Design flow - Waterfall vs spiral, Top-down vs Bottom up, Specification requirement, Types of Specification, System Design process, System level design issues- Soft IP vs Hard IP |
| **II** | Macro Design Process: Top level Macro Design, Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design process, System Integration with reusable macros. |
| **III** | Design for Testability Fundamentals: Faults in Digital circuits, Fault models ,Digital test pattern generation – ATPG, Roth's D-algorithm, Vector Simulation- ATPG Vectors, Formats, Compaction and Compression. |
| **IV** | Scan Architectures and testing- , Generic Boundary scan, Full integrated scan, Syndrome test band signature analysis. Built in Self Test (BIST):BIST concepts and test pattern generation |
| **V** | SoC Verification: Verification technology options, Verification methodology, Verification languages, Verification approaches and Verification plans, System level verification, Block level verification, Hardware/software co-verification and Static net list verification. |

**Text books:**

1. Prakash Rashinkar, Peter Paterson and Leena Singh, SoC Verification-Methodology and Techniques, .Kluwer Academic Publishers, 2001.

2. Michael Keating, Pierre Bricaud, Reuse Methodology manual for System-On-A-Chip

Designs, Kluwer Academic Publishers, second edition, 2001.

3. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Digital systems Testing and testable Design, Jaico Publishing House, 2001.

4. William K.Lam, Design Verification: Simulation and Formal Method based Approaches,Prentice Hall.2005

**Course Contents and Lecture Schedule**

| N0. | Topic | No. of lectures |
|---|---|---|
| **1** | **Module** | |
| 1.1 | System On Chip Design Process: A canonical SoC Design, | 2 |
| 1.2 | SoC Design flow - Waterfall vs spiral, Top-down vs Bottom up, Specification requirement, | 2 |
| 1.3 | Types of Specification, System Design process, System level design issues- Soft IP vs Hard IP | 2 |
| 2 | **Module II:** | |
| 2.1 | Macro Design Process: Top level Macro Design, | 2 |
| 2.2 | Macro Integration, Soft Macro productization, | 2 |
| 2.3 | Developing hard macros, Design issues for hard macros, | 2 |
| 2.4 | Design process,System Integration with reusable macros. | 1 |
| **3** | **Module III:** | |
| 3.1 | Design for Testability Fundamentals: Faults in Digital circuits, | 1 |
| 3.2 | Fault models ,Digital test pattern generation – ATPG, Roth's D-algorithm, | 1 |
| 3.3 | Vector Simulation- ATPG Vectors, Formats, Compaction and Compression. | 4 |

| | | |
|---|---|---|
| **4** | **Module IV:** | |
| 4.1 | Scan Architectures and testing- , Generic Boundary scan, Full integrated scan, | 3 |
| 4.2 | Syndrome test band signature analysis. | 3 |
| 4.3 | Built in Self Test (BIST):BIST concepts and test pattern generation | 4 |
| **5** | **Module V:** | |
| 5.1 | SoC Verification: Verification technology options, | 2 |
| 5.2 | Verification methodology, Verification languages, | 2 |
| 5.3 | Verification approaches and Verification plans, System level verification, Block level verification, Hardware/software co-verification and Static net list verification. | 2 |

**Model Question Paper**
**A P J Abdul Kalam Technological University**
**sixth Semester B Tech Degree Examination**
**Branch: Electronics and Communication Engg.**
**Course: SOC DESIGN**

**Time: 3 Hrs** **Max. Marks: 100**

**PART A**

Answer All Questions. Each question carry 3 marks

1. Outline the typical steps involved in the system design process of an SoC. How does this process ensure that the final design meets the specified requirements?

2. What are the advantages and disadvantages of integrating Soft IP versus Hard IP components?

3.Explain the challenges associated with integrating a macro into a larger system design.

4 Define the concept of soft macro productization.

5 Discuss the differences between single stuck-at 0 faults and stuck-at 1 faults.

6 What is ATPG (Automatic Test Pattern Generation)?

7 Describe the role of the Boundary Scan Register (BSR) in the boundary scan architecture.

8.How does full integrated scan differ from generic boundary scan?

9. What are the different Verification Description Languages (VDL) ?

10. Explain the significance of reuse in verification methodology.

## PART B

**Answer one question from each module. Each question carries 14 mark.**

11(a). Explain the differences between top-down and bottom-up design approaches in the context of SoC development. How do these approaches influence the overall design process? (9)

11(b)Explain why verification is crucial in each phase of the SoC design process. How does it ensure the reliability of the final product? (5)

**OR**

12(a) When would you prefer to use a Waterfall design flow over a Spiral design flow, and vice versa? Provide examples to support your answer. (9)

12(b) Discuss the challenges associated with integrating Soft IP and Hard IP into a cohesive SoC design. (5)

13(a) What strategies should be implemented to manage and maintain a library of reusable macros effectively? How can version control and documentation facilitate reuse? (7)

13(b) Identify and discuss the design issues specific to hard macros. How do these issues differ from those encountered in soft macros? (7)

**OR**

14(a) Outline the process of developing hard macros. What are the critical factors to consider during the conversion of a soft macro into a hard macro suitable for specific semiconductor technologies? (9)

14(b) Describe the tools and methodologies commonly used for physical design tasks associated with hard macros, such as floor planning, placement, routing, and timing closure. (5)

15.a) Explain the different types of fault models in the context of digital circuit testing. (9)

15(b)Discuss the importance of vector simulation in ATPG. How does vector simulation validate the effectiveness of generated test patterns? (5)

**OR**

16 a.) Explain Roth's D-algorithm. How does it generate test patterns to detect faults in digital circuits? (8)

b) Describe the Fault equivalence and Equivalence rules with example. (6)

17.(a) Explain pattern generation in BIST? What is an LFSR? Describe pattern generation using LFSR. (10)

17 (b) What is signature analysis, and how does it contribute to testing in digital systems? (4)

**OR**

18.(a).Design a weighted pseudo-random pattern generator with programmable weights 1/2, 1/4,11/32and 1/16. (10)

18(b).What is the significance of the BYPASS instruction in boundary scan? (4)

19.(a)Discuss the importance of System Level Verification. (10)

19.(b)Draw the block diagram of Hardware/Software Co-verification. (4)

**OR**

20. Explain verification strategies in SoC Design. (14)

| EVT 306 | DIGITAL SIGNAL PROCESSING | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:** This course aims to lay the foundational aspects of signals and systems in both continuous time and discrete time, in preparation for more advanced subjects in digital signal processing, image processing, communication theory and control systems and helps to understand the principles, algorithms and applications of DSP.

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO1** | Apply properties of signals and systems to classify them. |
| **CO2** | Apply transfer function to compute the LTI response to input signals. |
| **CO3** | Compute DFT and IDFT using DIT and DIF radix-2 FFT algorithms. |
| **CO4** | Illustrate the various FIR and IIR filter structures for the realization of the given system function. |
| **CO5** | Explain the architecture of DSP processor (TMS320C67xx) and the finite word length effects. |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | | 3 | | | | | | | 2 |
| **CO2** | 3 | 3 | 3 | | 3 | | | | | | | 2 |
| **CO3** | 2 | 2 | 2 | | 2 | | | | | | | 2 |
| **CO4** | 2 | 2 | 2 | | 2 | | | | | | | 2 |
| **CO5** | 2 | 2 | 2 | | 2 | | | | | | | 2 |

**Assessment Pattern**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|
| | 1 | 2 | |
| Remember K1 | 10 | 10 | 10 |
| Understand K2 | 20 | 20 | 30 |
| Apply K3 | 20 | 20 | 60 |
| Analyse K4 | | | |
| Evaluate | | | |
| Create | | | |

**Mark distribution**

| Total | CIE | ESE | ESE Duration |
|---|---|---|---|
| **Marks** | | | |
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1) : Apply properties of signals and systems to classify them**
1. Check whether the following systems are stable, causal, linear, and time-invariant
(a) y[n] = x[2n], (b) y(t) = x2(t) + 3, (c) y[n] = nx[n].

2. Plot (a) u(t-1) + u(1-t), (b) u(t-1) – u(t+1), (c) sinc(t/T), (d) r(t) – r(t-2) – 2u(t-2).

**Course Outcome 2 (CO2) : Apply transfer function to compute the LTI response to input signals.**

1. Give the frequency response of a first-order low pass filter. What is the 3-dB cut off frequency?
2. What is the significance of linear phase response?

**Course Outcome 3 (CO3) : Compute DFT and IDFT using DIT and DIF radix-2 FFT algorithms.**

1. Find the 8 point DFT of a real sequence x(n)={1,2,2,2,1,0,0,0,0} using Decimation in frequency algorithm?
2. Find out the number of complex multiplications require to perform an 1024 point DFT using(i)direct computation and (ii) using radix 2 FFT algorithm?

**Course Outcome 4 (CO4) : Illustrate the various FIR and IIR filter structures for the realization of the given system function.**

1. Obtain the direct form II and transpose structure of the filter whose transfer function is given below.

$$H(z)=\frac{0.44\,z^2+0.362\,z+0.02}{z^3+.4\,z^2+.18\,z-0.2}$$

2. Realize an FIR system with the given difference equation y(n)=x(n)-0.5x(n-1)+0.25x(n-2)+0.5x(n-3)-0.4x(n-4)+0.2x(n-5)

**Course Outcome 5 (CO5) : Explain the architecture of DSP processor (TMS320C67xx) and the finite word length effects**

1. Derive the variance of quantization noise in an ADC with step size Δ, assuming uniformly distributed quantization noise with zero mean ?
2. Bring out the architectural features of TMS320C67xx digital signal processor?

## SYLLABUS

| Module | Course contents |
|---|---|
| I | **Introduction to Continuous and discrete Time Signals** Definition of signal. Basic continous-time signals. Frequency and angular frequency, Basic operation on signals. Basic discrete-time signals - Frequency and angular frequency of discrete-time signals. Classification of continous-time & discrete- time signals: Periodic and Non-periodic signals, Even and Odd signals, Energy and power signals. |
| II | **Systems** System definition. Continuous-time and discrete-time systems. Properties – Linearity, Time invariance, Causality, Invertibility, Stability. Representation of systems using impulse response. |

| | |
|---|---|
| | Linear time invariant systems:- LTI system definition. Response of a discrete-time LTI system and the Convolutional Sum. Circular convolution, Linear convolution through circular convolution Correlation of discrete-time signals |
| **III** | **Frequency analysis of signals** Fourier transform of continuous-time and discrete-time signals. Parsevals theorem. Interpretation of Spectra. The sampling theorem(Proof not needed). Frequency aliasing due to sampling. Need for anti-aliasing filters. Discrete Time Fourier Transforms – Properties. Discrete Fourier Transform – Properties -DFT as a linear transformation, IDFT ,FFT-Radix-2 DIT and DIF algorithms. FFT Algorithms for IDFT |
| **IV** | **Digital Filters Digital FIR Filter** Transfer function - Difference equation, Linear phase FIR filter, Concept of windowing, Direct form and cascade realization. Digital IIR Filters – Transfer function, Difference equation. Direct and parallel Structures. Design of analogue Butterworth filters, Analog frequency transformations, Impulse invariance method. Bilinear transformation, Analog prototype to digital transformations. |
| **V** | **Computer architecture for signal processing**<br>Harvard Architecture, pipelining, MAC, Introduction to TMS320C67xx digital signal processor, Functional Block Diagram. Finite word length effects in DSP systems: Introduction (analysis not required), fixed-point and floating-point DSP arithmetic, ADC quantization noise, Finite word length effects in IIR digital filters: coefficient quantization errors. Finite word length effects in FFT algorithms: Round off errors. |

**Texts/References**


1. A Anand Kumar, Signals and systems, PHI learning

2. Sanjay Sharma, Signals and systems

3. Simon Haykin, Barry Van Veen, Signals and systems, John Wiley

4. Hwei P.Hsu, Theory and problems of signals and systems, Schaum Outline Series, MGH.

5. Proakis, J.G. & Manolakis, D.G., “Digital Signal Processing: Principles, Algorithms,& Applications”,3/e Prentice Hall of India, 1996.

6. Mitra, S.K., “Digital Signal Processing: A Computer-Based Approach”, McGraw Hill, NY, 1998

7. Monson H Hayes, Schaums outline: Digital Signal Processing

**Course Contents and Lecture Schedule**

| N0. | Topic | No. of lectures |
|---|---|---|
| **1** | **Module: Introduction to Continuous and discrete Time Signals** | |
| 1.1 | Definition of signal. Basic continous-time signals. Frequency and angular frequency, Basicoperation on signals. | 2 |
| 1.2 | Basic discrete-time signals - Frequency and angular frequency of discrete-time signals. | 2 |
| 1.3 | Classification of continous-time & discrete- time signals: Periodic and Non-periodic signals, Even and Odd signals, Energy and power signals. | 2 |
| 2 | Module : Systems | |
| 2.1 | System definition. Continuous-time and discrete-time systems. | 2 |
| 2.2 | Properties – Linearity, Time invariance, Causality, Invertibility, Stability. Representation of systems using impulse response. | 2 |
| 2.3 | Linear time invariant systems:- LTI system definition. Response of a discrete-time LTI system and the Convolutional Sum. | 2 |
| 2.4 | Circular convolution, Linear convolution through circular convolution Correlation of discrete-time signals. | 1 |
| **3** | **Module 3 : Frequency analysis of signals** | |
| 3.1 | Fourier transform of continuous-time and discrete-time signals. Parsevals theorem. | 1 |
| 3.2 | Interpretation of Spectra. The sampling theorem(Proof not needed). Frequency aliasing due to sampling. Need for anti-aliasing filters. | 1 |
| 3.3 | Discrete Time Fourier Transforms – Properties. Discrete Fourier Transform – Properties -DFT as a linear | 4 |

| | | |
|---|---|---|
| | transformation, IDFT ,FFT-Radix-2 DIT and DIF algorithms. FFT Algorithms for IDFT | |
| **4** | **Module 4: Digital Filters** | |
| 4.1 | Digital FIR Filter: Transfer function - Difference equation, Linear phase FIR filter, Concept of windowing, Direct form and cascade realization. | 3 |
| 4.2 | Digital IIR Filters – Transfer function,Difference equation. Direct and parallel Structures. | 3 |
| 4.3 | Design of analogue Butterworth filters, Analog frequency transformations, Impulse invariance method. Bilinear transformation, Analog prototype to digital transformations. | 4 |
| **5** | **Module Computer architecture for signal processing:** | |
| 5.1 | Harvard Architecture, pipelining, MAC, Introduction to TMS320C67xx digital signal processor, Functional Block Diagram. | 2 |
| 5.2 | Finite word length effects in DSP systems: Introduction (analysis not required), fixed-point and floating-point DSP arithmetic, ADC quantization noise, | 2 |
| 5.3 | Finite word length effects in IIR digital filters: coefficient quantization errors. Finite word length effects in FFT algorithms: Round off errors. | 2 |

**Simulation Assignments**

The following simulations to be done in Scilab/ Matlab/ LabView/GNU Octave:

1. Consider a signal given by x(n)=[1,1,1,1].

1. Compute the DTFT of the given sequence and plot its magnitude and phase
2. Compute the 4 point DFT of the above signal and plot its magnitude and phase
3. Compare the above plots and obtain the relationship?

2. Zero pad the sequence x(n) by 4 and compute the 8 point DFT and find the corresponding magnitude and phase plots. Compare the spectra with that in (b) and comment on it.

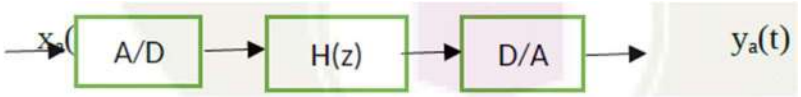
3. The first five values of the 8 point DFT of a real valued sequence x(n) are given by {0.25, 0.125-j0.3, 0, 0.125-j0.06, 0.5}. Determine the DFT of each of the following sequences using properties. Hint :IDFT may not be computed.

1. x1(n)=x((2-n))8
2. x3(n)=x2(n)
3. x4(n)=x(n)e jπn/N) in/4

4. a) Develop a function to implement the over-lap add method using circular convolution operation. The format should be function [y]=overlappadd(x,h,N), where y is the output sequence, x is the input sequence and N is the block - length>=2*Length(h)-1.

1. Incorporate the radix-2 FFT implementation in the above function to obtain a high speed overlap add block convolution routine. Choose N=8. Hint :choose N=2k

5. Design a low pass digital filter to be used in the given structure




to satisfy the following requirements. Sampling rate of 8000 samples/second, Pass band edge of 1500Hz with a ripple of 3dB, Stopband edge of 2000Hz with attenuation of 40 dB, Equiripple passband but monotonic stopband. (Use impulse invariance technique)

1. Choose T=1 s for impulse invariance and determine the system function H(z) in parallel form.Plot the log-magnitude response in dB and impulse response h(n)
2. Choose T=1/8000 s and repeat the same procedure. Compare this design with that in (a) and comment on the effect of T on the impulse invariant design?

6. A filter is described by the following difference equation:
16y(n)+12y(n-1)+2y(n-2)-4y(n-3)-y(n-4) = x(n)-3x(n-1)+11x(n-2)-27x(n-3)+18x(n-4)

1. Determine the Direct form filter structure
2. Using the Direct form structure, obtain the cascade form filter structure

7. Consider a signal given by x(n)=(0.5)nu(n). Decimate the signal by a factor 4 and plot the output in time domain and frequency domain?

1. Interpolate the signal by a factor of 4 and plot the output in time domain and frequency domain?

2. Compare the spectra and obtain the inference?

**Model Question Paper**
**A P J Abdul Kalam Technological University**
**sixth Semester B Tech Degree Examination**
**Branch: Electronics and Communication Engg.**
**Course: DIGITAL SIGNAL PROCESSING**

**Time: 3 Hrs** **Max. Marks: 100**

**PART A**

Answer All Questions. Each question carry 3 marks

1 Differentiate between energy and power signal with example.

2 Find the even and odd components of x(t) = ejt.

3 Derive a relationship between input and output for a discrete LTI system

4 Find the circular convolution of two sequences x1(n)={1, 2,-2,1,3},x2(n)={2,-1,3,1,1}

5 Illustrate the basic butterfly computation used in decimation in time radix-2 FFT algorithm ?

6 Bring out the computational advantage of performing an N-point DFT using radix-2 FFT compared to direct method?

7 Determine the frequency response of a linear phase FIR filter given by the difference equation y(n)=0.15x(n)+0.25x(n-1)+x(n-3). Also find the phase delay

8.An all pole analog filter is given by the transfer function H(s)=1 /(s2+5s+6). Find out the transfer function H(z) of the equivalent digital filter using impulse invariance method. Use T=1s

9. Differentiate between Harvard architecture and Von-Nuemann Architecture used in processors?

10. Express the fraction 7/8 and -7/8 in sign-magnitude, two's compliment and one's compliment format?

PART B

Answer one question from each module. Each question carries 14 mark.

11(A) Determine whether or not the signal x(t) = cos t + sinp$\sqrt{\ }$2t is periodic. If periodic, determine its fundamental period. (7)

11(B)Define, sketch and list the properties of continuous time impulse function (7)

OR

12(A) Determine whether the signal x(t) = e-2tu(t) is energy signal, power signal or neither. (7)

12(B) Define unit step function and plot u(t + 2) - u(t - 2). (7)

13(A) Given the sequence x(n) ={ 1,2,1,1,3}, $-1 \leq n \leq 3$. Sketch

- x(-n + 2),
- x(n=2) (7)

13B How will you perform linear convolution using circular convolution? Find the linear convolution of the given sequences x(n) = {2, 9,7, 4} and h(n) = {1, 3, 1, 2} using circular convolution? (7)

OR

14 A system has an input-output relation given by y(n) = T{x(n)} = nx(n). Determine whether the system is

a)Memoryless

b)Causal

c) Linear

d) Time invariant

e)Stable (14)

15.a) Compute the 8 point DFT of x(n) = {2,1,-1,3,5,2,4,1} using radix-2 decimation in time FFT algorithm. (9)

b)Bring out how a 2N point DFT of a 2N point sequence can be found using the computation of a single N point DFT. (5)

OR

16 a.) Find the 8 point DFT of a real sequence x(n)={1,2,2,2,1,0,0,0,0} using radix-2 decimation in frequency algorithm (9)

b) Bring out how N-point DFT of two real valued sequences can be found by computing a single N-point DFT. (5)

17.a. Design a linear phase FIR low pass filter having length M = 15 and cut-off frequency $\omega c = \pi /6$. Use a Hamming window. (10)

b.Prove that if z1 is a zero of an FIR filter, then 1/z1 is also a zero? (4)

OR

18. a. Design a digital Butterworth low pass filter with $\omega p = \pi /6$, $\omega s = \pi/4$, minimum pass band gain = -2 dB and minimum stop band attenuation = 8 dB. Use bilinear transformation.(Take T = 1s) (10)

b. What is warping effect in bilinear transformation and how it can be eliminated? (4)

19.a.With the help of a functional block diagram, explain the architecture of TMS320C67xx DSP processor? (10)

b.What are the prominent features of TMS320C67xx compared to its predecessors ? (4)

OR

20.a)Explain how to minimize the effect of finite word length in IIR digital filters? (7)

b)Explain the roundoff error models used in FFT algorithms? (7)

| ECT302 | ELECTROMAGNETICS | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:** This course aims to impart knowledge on the basic concepts of electric and magnetic fields and its applications.

**Prerequisite:** MAT102 Vector Calculus

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| CO 1 K2 | To summarize the basic mathematical concepts related to electromagnetic vector fields. |
| CO 2 K3 | Analyse Maxwell's equation in different forms and apply them to diverse engineering problems. |
| CO3 K3 | To analyse electromagnetic wave propagation and wave polarization |
| CO4 K3 | To analyse the characteristics of transmission lines and solve the transmission line problems using Smith chart. |
| CO5 K3 | To analyse and evaluate the propagation of EM waves in Wave guides. |

**Mapping of course outcomes with program outcomes**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 1 | 1 | | | | | | | | 2 |
| **CO2** | 3 | 3 | 1 | 1 | | | | | | | | 2 |
| **CO3** | 3 | 3 | 1 | 1 | | | | | | | | 2 |
| **CO4** | 3 | 3 | 1 | 1 | | | | | | | | 2 |
| **CO5** | 3 | 3 | 1 | 1 | | | | | | | | 2 |

**Assessment Pattern**

| Bloom's Category | | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|---|
| | | 1 | 2 | |
| Remember | K1 | | | |
| Understand | K2 | 20 | 20 | 40 |
| Apply | K3 | 30 | 30 | 60 |
| Analyse | | | | |
| Evaluate | | | | |
| Create | | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1): To summarize the basic mathematical concepts related to electromagnetic vector fields. (K2)**

1. State and explain divergence theorem. Give a geometrical explanation.

2. Find the curl of the vector A $=2r\cos\phi\, a_\rho + r\, a_\phi$ in cylindrical coordinates

3. Show that curl grad **F** and div curl **F** are identically zero.

4. Show that $V = \frac{1}{4\pi\varepsilon_0}\frac{Q}{r}$ where $r = (x^2 + y^2 + z^2)^{1/2}$ satisfies Laplace's equation.

**Course Outcome 2 (CO2): Analyse Maxwell's equation in different forms and apply them to diverse engineering problems. (K3)**

1. State and explain Maxwell's equations in the integral and differential forms.

2. Derive the solution of uniform plane wave in lossy dielectric medium.

**Course Outcome 3 (CO3): To analyse electromagnetic wave propagation and wave polarization (K3)**

1. Derive an expression for reflection coefficient of a plane wave under oblique incidence with parallel polarization at a dielectric interface.

2. Explain wave polarization and different polarisation with example.

3. Derive the expression for Brewster angle for parallel polarised wave.

**Course Outcome 4 (CO4): To analyse the characteristics of transmission lines and solve the transmission line problems using Smith chart. (K3)**

1. A transmission line of length 0.2 λ and characteristic impedance 100Ω is terminated with a load impedance of 50+200j . Find input impedance, reflection coefficient at load end, reflection coefficient at the input end and VSWR.

2. A lossless transmission line has a characteristic impedance of 50Ω and phase constant of 3 Rad/ m at 100 MHz . Find Inductance per meter and Capacitance per meter of the transmission line .

3. A 50 + j200 Ω load is connected to a 100Ω lossless transmission line . Using Smith chart , find i. Reflection coefficient at load ii. VSWR

**Course Outcome 5 (CO5): To analyse and evaluate the propagation of EM waves in Wave guides.(K3)**

1. For TE10 mode of propagation in a rectangular wave guide, with length 8cm and

6 cm respectively , find the following when frequency of operation is 6 GHz .

i. Cut off frequency

ii. Cut off wavelength

iii. Guide wavelength

iv. Phase constant

v. Phase velocity

vi. Group velocity

vii. Wave impedance

2. A rectangular wave guide has a dimension of 3cm x 5cm , and is operating at a frequency of 10 GHz . Calculate the cutoff wavelength, cutoff frequency , guide wavelength , phase velocity and group velocity . and the wave impedance for TE10 mode.

3. Derive the expression for Electric and magnetic field intensities for TM mode of propagation of rectangular waveguide.

## SYLLABUS

**MODULE 1 :**

Introduction to Electromagnetic Theory. Review of vector calculus- curl, divergence gradient. Rectangular, cylindrical and spherical coordinate systems. Expression of curl divergence and Laplacian in cartesian, cylindrical and spherical coordinate system. Electric field and magnetic field, Review of Coulomb's law, Gauss law and Amperes current law. Poisson and Laplace equations, Determination of E and V using Laplace equation.

**MODULE 2 :**

Derivation of capacitance and inductance of two wire transmission line and coaxial cable. Energy stored in Electric and Magnetic field. Displacement current density, continuity equation. Magnetic vector potential. Relation between scalar potential and vector potential. Maxwell's equation from fundamental laws. Boundary condition of electric field and magnetic field from Maxwells equations.Solution of wave equation.

**MODULE 3 :**

Propagation of plane EM wave in perfect dielectric, lossy medium, good conductor, media-attenuation, phase velocity, group velocity, skin depth. Reflection and refraction of plane electromagnetic waves at boundaries for normal & oblique incidence (parallel and perpendicular polarization), Snell's law of refraction, Brewster angle.

**MODULE 4 :**

Power density of EM wave, Poynting vector theorem. Polarization of electromagnetic wave-linear, circular and elliptical polarisation.

Uniform lossless transmission line - line parameters.Transmission line equations, Voltage and Current distribution of a line terminated with load .Reflection coefficient and VSWR. Derivation of input impedance of transmission line.

**MODULE 5 :**

Transmission line as circuit elements (L and C). Development of Smith chart - calculation of line impedance and VSWR using smith chart.

The hollow rectangular wave guide –modes of propagation of wave-dominant mode, group velocity and phase velocity -derivation and simple problems only

**Text Books**

1. John D. Kraus, Electromagnetics, 5/e, TMH, 2010.
2. Mathew N O Sadiku, Elements of Electromagnetics, Oxford University Press, 6/e, 2014.
3. William, H. Hayt, and John A. Buck. Engineering Electromagnetics. McGraw-Hill, 8/e McGraw-Hill, 2014.

**Reference Books**


1. Edminister, "Schaum's Outline of Elctromagnetics", 4/e, McGraw-Hill, 2014.
2. Jordan and Balmain , Electromagnetic waves and Radiating Systems, PHI, 2/e,2013
3. Martin A Plonus , Applied Electromagnetics, McGraw Hill, 2/e,1978.
4. Nannapaneni Narayana Rao, Elements of Engineering Electromagnetics, Pearson, 6/e, 2006.
5. Umran S. Inan and Aziz S. Inan, Engineering Electromagnetics, Pearson, 2010.


**Course Contents and Lecture Schedule**

| No | Topic | No. of Lectures |
|---|---|---|
| **1** | **Module 1** | |
| 1.1 | Introduction to Electromagnetic Theory. Review of vector calculus- curl, divergence gradient. | 3 |
| 1.2 | Rectangular, cylindrical and spherical coordinate systems. Expression of curl divergence and Laplacian in cartesian , cylindrical and spherical coordinate system. | 3 |
| 1.3 | Electric field and magnetic field.Review of Coulomb's law , Gauss law and Amperes current law. | 2 |
| 1.4 | Poisson and Laplace equations, Determination of E and V using Laplace equation. | 2 |
| **2** | **Module 2** | |
| 2.1 | Derivation of capacitance and inductance of two wire transmission line and coaxial cable. | 2 |
| 2.2 | Energy stored in Electric and Magnetic field. | 1 |
| 2.3 | Displacement current density, continuity equation. Magnetic vector potential. Relation between scalar potential and vector potential. | 3 |
| 2.4 | Maxwell's equation from fundamental laws. | 2 |
| | Boundary condition of electric field and magnetic field from Maxwell's equations. | 1 |
| 2.5 | Solution of wave equation | 1 |
| **3** | **Module 3** | |
| 3.1 | Propagation of plane EM wave in perfect dielectric, lossy medium, good conductor, media-attenuation, phase velocity, group velocity, skin depth. | 4 |
| 3.2 | Reflection and refraction of plane electromagnetic waves at boundaries for normal & oblique incidence (parallel and perpendicular polarization), Snell's law of refraction, Brewster angle. | 4 |
| **4** | **Module 4** | |

| | | |
|---|---|---|
| 4.1 | Power density of EM wave, Poynting vector theorem. | 2 |
| 4.2 | Polarization of electromagnetic wave-linear, circular and elliptical polarisation. | 2 |
| 4.3 | Uniform lossless transmission line - line parameters. Transmission line equations | 3 |
| 4.4 | Voltage and Current distribution of a line terminated with load .Reflection coefficient and VSWR.Derivation of input impedance of transmission line. | 3 |
| **5** | **Module 5** | |
| 5.1 | Transmission line as circuit elements (L and C). | 1 |
| 5.2 | Development of Smith chart - calculation of line impedance and VSWR using smith chart. | 3 |
| 5.3 | The hollow rectangular wave guide –modes of propagation of wave-dominant mode, group velocity and phase velocity -derivation and simple problems only | 4 |

**Assignments:**

**Model Question paper**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

SIXTH SEMESTER B.TECH DEGREE EXAMINATION, (**Model Question Paper)**

**Course Code: ECT302**

**Course Name: ELECTROMAGNETICS**

Max. Marks: 100 Duration: 3 Hours

**PART A**

Answer ALL Questions. Each Carries 3 mark.

| | | |
|---|---|---|
| 1 | Define Curl of a vector field. Explain its physical significance. | K2 |
| 2 | Obtain Coulomb's law from Gauss' law | K2 |
| 3 | Write Poisson's and Laplace's Equation with applications | K1 |
| 4 | A Parallel plate capacitor with plate area of $5cm^2$ and a plate separation of 3mm has a voltage $50\sin 10^3 t$ Volt applied to its plates. Calculate the displacement current assuming $\varepsilon = 2\varepsilon_0$. | K3 |
| 5 | List all Maxwell's equations in integral form | K1 |

| | | | |
|---|---|---|---|
| 6 | Explain the significance of skin depth. | | K2 |
| 7 | What is Snell's law? | | K1 |
| 8 | What is wave polarisation? What are the different types of polarisation? | | K1 |
| 9 | State the relation between standing wave ratio and reflection coefficient. | | K1 |
| 10 | How a quarter wave dissipationless line can be used for impedance matching?. | | K2 |

## PART – B

Answer one question from each module; each question carries 14 marks.

### Module - I

| | | | |
|---|---|---|---|
| 11 a. | Derive the equation for curl of a vector field in Cartesian co-ordinate system. | 7 | CO1 K2 |
| b. | A Spherical volume charge distribution is given by<br>$p = p_0(1 - \frac{r^2}{a^2}); r \leq a$<br>$p = 0; r > a$<br>Find the electric field intensity E; i) inside and ii) outside the charge distribution | 7 | CO1 K3 |

**OR**

| | | | |
|---|---|---|---|
| 12 | Interpret the following<br>i) $\nabla \times B = \mu_0 J$ ii) $\nabla \times E = 0$ where B and J stands for magnetic flux density and electric current density | 7 | CO1 K3 |
| b. | Apply Ampere's circuital law to the case of an infinitely long coaxial cable carrying a uniformly distributed total current I. Compute the magnetic field intensity existing in different parts of the cable. | 7 | CO1 K3 |

### Module - II

| | | | |
|---|---|---|---|
| 13 a. | Derive the expression of capacitance of two wire transmission line. | 7 | CO2 K2 |
| b. | Show that the energy stored in a system of n point charges is given by | 7 | |

$W_E = \frac{1}{2}\sum_{i=1}^{n} Q_i V_i$ where $V_i$ is the potential of the point charge $Q_i$. CO2 K3

**OR**

14a Define vector magnetic potential and show that $B = \nabla \times A$, where B is the magnetic flux density and A is the vector magnetic potential at any point. 7 CO2 K2

b State and prove boundary conditions for E and H in accordance with Maxwell's equations. 7 CO2 K2

**Module - III**

15 a. Derive the expression for reflection coefficient for a wave of perpendicular polarization , travelling from one medium to another at oblique incidence . 7 CO3 K2

b. In a lossy dielectric medium,characteristic impedance of the medium is 173 +j100 Ω , Expression of Magnetic field of a plane wave is given by $10\, e^{-\alpha x}\cos(\omega t - 0.5x)a_z$ A/m . Find 7 CO3 K3

i. Direction of propagation

ii. Loss tangent

iii. Attenuation constant

iv. Phase constant

v. Skin depth

**OR**

16 a Derive continuity equation from fundamental laws. 7 CO3 K2

b Find the skin depth, δ at a frequency of 1.6 MHz in aluminium, where $\sigma$=38.2MS/m and $\mu_r$= 1. Also find the propagation constant, γ and the wave

| | | | |
|---|---|---|---|
| | velocity v . | 7 | CO3 K3 |

**Module - IV**

| | | | |
|---|---|---|---|
| 17a | Derive the equation for transmission and reflection coefficients of an electromagnetic wave incident normally on the boundary between two different regions. | 7 | CO4 K2 |
| b | Derive an expression for net outward power flow associated with an electromagnetic wave, from a surface. | 7 | CO4 K2 |

**OR**

| | | | |
|---|---|---|---|
| 18 a. | Derive standard Transmission line equations. | 7 | CO4 K2 |
| b. | Given two dielectric media,the first medium is free space and the second medium has $\varepsilon_2 = 4\varepsilon_0$ and $\mu = \mu_0$. Find the reflection coefficient for oblique incidence at $\theta_1 = 30^o$ for i) perpendicular polarisation and ii) parallel polarisation | 7 | CO4 K3 |

**Module - V**

| | | | |
|---|---|---|---|
| 19 a. | A rectangular wave guide has a dimension of 3cm x 5cm , and is operating at a frequency of 10 GHz . Calculate the cutoff wavelength, cutoff frequency , guide wavelength , phase velocity and group velocity . and the wave impedance for TE10 mode. | 7 | CO5 K3 |
| b. | At a frequency of 80 MHz, a lossless transmission line has a characteristic impedance of 300Ω and a wavelength of 2.5m. Find:<br>i) L ii) C iii) If the line is terminated with a parallel combination of 200Ω and 5pF, determine the reflection co-efficient and the standing wave ratio. | 7 | CO5 K3 |

**OR**

| | | | |
|---|---|---|---|
| 20 a | A 50 + j200 Ω load is connected to a 100Ω lossless transmission line . Using smith chart , find | 7 | |

| | | | |
|---|---|---|---|
| | i. Reflection coefficient at load ii. VSWR iii. Load admittance | | CO5 K3 |
| b | Derive the expression for Electric and magnetic field intensities for TM mode of propagation of rectangular waveguide. | 7 | CO5 K2 |

| ECT305 | ANALOG AND DIGITAL COMMUNICATION | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 3 | 1 | 0 | 4 |

**Preamble:** This course aims to develop analog and digital communication systems.

**Prerequisite**: MAT 204 Probability, Random Process and Numerical Methods

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO 1** | Explain the existent analog communication systems. |
| **CO 2** | Apply the concepts of random processes to LTI systems. |
| **CO 3** | Apply waveform coding techniques in digital transmission. |
| **CO 4** | Apply GS procedure to develop digital receivers. |
| **CO 5** | Apply equalizer design to counteract ISI. |
| **CO 6** | Apply digital modulation techniques in signal transmission. |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO 1** | 3 | 3 | | | | | | | | | | |
| **CO 2** | 3 | 3 | 2 | 3 | 3 | | | | | | | |
| **CO 3** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |
| **CO 4** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |
| **CO 5** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |
| **CO 6** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |

**Assessment Pattern**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|
| | 1 | 2 | |
| Remember | 10 | 10 | 20 |
| Understand | 30 | 30 | 60 |
| Apply | 10 | 10 | 20 |
| Analyse | | | |
| Evaluate | | | |
| Create | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

## Course Level Assessment Questions

**Course Outcome 1 (CO1): The existent analog communication system**

1. What are the needs for analog modulation
2. Give the mathematical model of FM signal and explain its spectrum.

**Course Outcome 2 (CO2): Application of random processes**

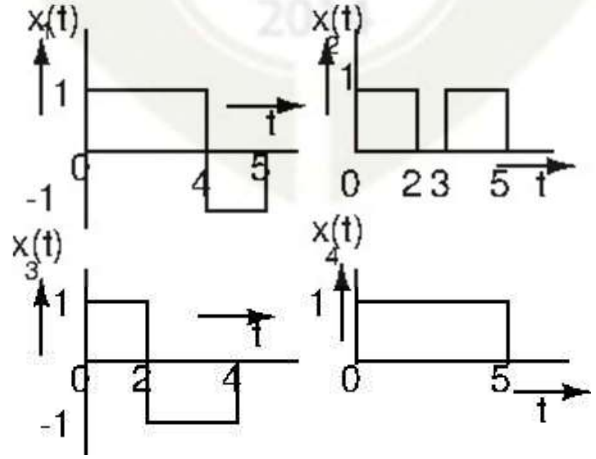
1. Compute the entropy of a Gaussian random variable.
2. A six faced die is thrown by a player. He gets Rs. 100 if face 6 turns up, loses Rs. 20 if face 3 or 4 turn up, gets Rs. 50 if face 5 turns up and loses Rs 10 if face 1 or 2 turn up. Draw the pdf and CDF for the random variable. Check if it is profitable based on statistical expectation.

**Course Outcome 3 (CO3): Waveform coding**

1. Compute the A and mu law quantized values of a signal that is normalized to 0.8 with A=32 and mu=255.
2. Design a 3-tap linear predictor for speech signals with the autocorrelation vector [0.95,0.85,0.7,0.6] , based on Wiener-Hopf equation. Compute the minimum mean square error.

**Course Outcome 4 (CO4): G-S Procedure and effects in the channel**

1. Apply G-S procedure on the following signals and plot their signal space.



2. Derive the Nyquist criterion for zero ISI.

**Course Outcome 5 (CO5): Digital modulation**

1. Give the mathematical model of a BPSK signal and plot its signal constellation.
2. Draw the BER-SNR plot for the BPSK system

## SYLLABUS

**Module 1 Analog Communication**

Block diagram of a communication system. Need for analog modulation. Amplitude modulation. Equation and spectrum of AM signal. DSB-SC and SSB systems. Block diagram of SSB transmitter and receiver. Frequency and phase modulation. Narrow and wide band FM and their spectra. FM transmitter and receiver.

**Module 2 Review of Random Variables and Random Processes**

Review of random variables – both discrete and continuous. CDF and PDF, statistical averages. (Only definitions, computations and significance) Entropy, differential entropy. Differential entropy of a Gaussian RV. Conditional entropy, mutual information.

Stochastic processes, Stationarity. Conditions for WSS and SSS. Autocorrelation and power spectral density. LTI systems with WSS as input.

**Module 3 Source Coding**

Source coding theorems I and II (Statements only). Waveform coding. Sampling and Quantization. Pulse code modulation, Transmitter and receiver. Companding. Practical 15 level A and mu-law companders. DPCM transmitter and receiver. Design of linear predictor. Wiener-Hopf equation. Delta modulation. Slope overload.

**Module 4 G-S Procedure and Effects in the Channel**

Gram-Schmitt procedure. Signal space.

Baseband transmission through AWGN channel. Mathematical model of ISI. Nyquit criterion for zero ISI. Signal modeling for ISI, Raised cosine and Square-root raised cosine spectrum, Partial response signalling and duobinary coding. Equalization. Design of zero forcing equalizer.

Vector model of AWGN channel. Matched filter and correlation receivers. MAP receiver, Maximum likelihood receiver and probability of error.

Capacity of an AWGN channel (Expression only) -- significance in the design of communication schemes.

**Module 5 Digital Modulation Schemes**

Digital modulation schemes. Baseband BPSK system and the signal constellation. BPSK

transmitter and receiver. Base band QPSK system and Signal constellations. Plots of BER Vs SNR with analysis. QPSK transmitter and receiver. Quadrature amplitude modulation and signal constellation.

**Text Books**

1. "Communication Systems", Simon Haykin, Wiley.
2. "Digital Communications: Fundamentals and Applications", Sklar, Pearson.
3. "Digital Telephony", John C. Bellamy, Wiley

**References**

1. "Principles of Digital Communication," R. Gallager, Oxford University Press
2. "Digital Communication", John G Proakis, Wiley.

**Course Contents and Lecture Schedule**

| No | Topic | No. of Lectures |
|---|---|---|
| **1** | **Analog Communication** | |
| 1.1 | Block diagram of communication system, analog and digital systems , need for modulation | 2 |
| 1.2 | Amplitude modulation, model and spectrum and index of modulation | 2 |
| 1.3 | DSB-SC and SSB modulation. SSB transmitter and receiver | 2 |
| 1.4 | Frequency and phase modulation. Model of FM, spectrum of FM signal | 2 |
| **2** | **Review of Random Variables** | |
| 2.1 | Review of random variables, CDF and PDF, examples | 2 |
| 2.2 | Entropy of RV, Differential entropy of Gaussian RV, Expectation, conditional expectation, mutual information | 4 |
| 2.3 | Stochastic processes, Stationarity, WSS and SSS. Autocorrelation and power spectral density. Response of LTI systems to WSS | 3 |
| **3** | **Source Coding** | |
| 3.1 | Source coding theorems I and II | 1 |
| 3.2 | PCM,Transmitter and receiver, companding Practical A and mu law companders | 4 |
| 3.3 | DPCM, Linear predictor, Wiener Hopf equation | 3 |
| 3.4 | Delta modulator | 1 |

| | | |
|---|---|---|
| **4** | **GS Procedure and Channel Effects** | |
| 4.1 | G-S procedure | 3 |
| 4.2 | ISI, Nyquist criterion, RS and SRC, PR signalling and duobinary coding | 3 |
| 4.3 | Equalization, design of zero forcing equalizer | 3 |
| 4.4 | Vector model of AWGN channel, Correlation receiver, matched filter | 4 |
| 4.5 | MAP receiver, ML receiver, probability of error | 1 |
| 4.6 | Channel capacity, capacity of Gaussian channel, Its significance in design of digital communication schemes | 2 |
| **5** | **Digital Modulation** | |
| 5.1 | Need of digital modulation in modern communication. | 1 |
| 5.2 | Baseband QPSK system, signal constellation. Effect of AWGN, probability of error (with derivation). BER-SNR curve, QPSK transmitter and receiver. | 4 |
| 5.3 | QAM system | 1 |

**Model Question Paper**

**A P J Abdul Kalam Technological University**

Fifth Semester B Tech Degree Examination Branch:

Electronics and Communication

**COURSE: ECT 305 ANALOG AND DIGITAL COMMUNICATION**

**Time: 3 Hrs** **Max. Marks: 100**

## PART A

*Answer All Questions*

| | | |
|---|---|---|
| 1 | Explain the need for modulation | (3)*K2* |
| 2 | Plot the spectrum of an FM signal | (3)*K2* |
| 3 | In a game a six faced die is thrown. If 1 or 2 comes the player gets Rs 30, if 3 or 4 the player gets Rs 10, if 5 comes he loses Rs. 30 and in the event of 6 he loses Rs. 100. Plot the CDF and PDF of gain or loss | (3) *K3* |
| 4 | Give the conditions for WSS | (3)*K2* |
| 5 | Compute the step size for a delta modulator without slope overload if the input is $A\cos 2\pi 120t$ | (3)*K3* |
| 6 | State source coding theorems I and II | (3)*K1* |
| 7 | Give the Nyquist criterion for zero ISI. | (3)*K1* |
| 8 | Give the mathematical model of ISI | (3)*K2* |
| 9 | Plot BER against SNR for a BPSK system | (3)*K2* |
| 10 | Draw the signal constellation of a QPSK system with and without AWGN. | (3)*K3* |

## PART B

*Answer one question from each module. Each question carries 14 mark.*

### Module I

| | | |
|---|---|---|
| 11(A) | Give the model of AM signal and plot its spectrum | (10)*K2* |
| 11(B) | If a sinusoidal is amplitude modulated by the carrier $5\cos 2\pi 300t$ to a depth of 30 %, compute the power in the resultant AM signal. | (4)*K3* |

**OR**

| | | |
|---|---|---|
| 12(A) | Explain how SSB is transmitted and received. | (10)*K2* |
| 12(B) | Compute the bandwidth of the narrow band FM signal with modulating signal frequency of $1kHz$ and index of modulation 0.3 | (4) *K3* |

### Module II

| | | |
|---|---|---|
| 13(A) | Compute the entropy of Gaussian random variable. | (10)*K3* |
| 13(B) | Give the relation between autocorrelation and power spectral density of a WSS. | (4)*K2* |

**OR**

| | | |
|---|---|---|
| 14(A) | Test whether the random process $X(t) = A\cos 2\pi ft + \theta$ is WSS if $\theta$ is uniformly distributed in the interval $[-\pi, \pi]$ | (10)*K3* |
| 14(B) | Explain mutual information. Give its relation with self information. | (4)*K2* |

### Module III

| | | |
|---|---|---|
| 15(A) | A WSS process with autocorrelation $RX(\tau) = e^{-\alpha\lvert\tau\rvert}$ is applied to an LTI system with impulse response $h(t) = e^{-\beta t}$ with $\lvert\alpha\rvert > 0$ and $\lvert\beta\rvert > 0$. Find the output power spectral density | (10)K3 |
| 15(B) | Give the conditions for stationarity in the strict sense. | (4)*K2* |

**OR**

16(A) Find an orthonormal basis set fot the set of signals (7)*K3*

$$s_1(t) = A\sin(2\pi f_0 t); \qquad 0 \le t \le T$$

and

$$s_2(t) = A\cos(2\pi f_0 t); \qquad 0 \le t \le T$$

where $f_0 = \frac{m}{T}$ where m is an integer.

16(B) Plot the above signal constellation and draw the decision region on it. Compute the probability of error. (7)*K3*

**Module IV**

17(A) Compute the probability of error for maximum likely hood detection of binary transmission. *(8)K3*

17(B) Explain the term matched filter. Plot the BER-SNR curve for a matched filter receiver (6)*K2*

**OR**

18(A) Design a zero forcing equalizer for the channel that is characterized by the filter taps *{*1,0.7,0.3*}* (8)*K3*

18(B) Explain partial rsponse signaling (6)*K2*

**Module V**

19 For a shift keying system defined by $s(t) = A_c\, k\sin(2\pi f_c t) \pm A_c k\cos(2\pi f_c t)$ plot the signal constellation. Compute the probability of error. (14)*K3*

**OR**

20(A) Derive the probability of error for a QPSK system with Gray coding. *(10)K3*

20(B) Draw the BER-SNR plot for a QPSK system (4)*K3*

**ECT 305 Analog and Digital Communication Simulation Assignments**

The following simulation assignments can be done with Python/MATLAB/ SCILAB/LabVIEW The following simulations can be done in MATLAB, Python,R or LabVIEW.

## 1 A-Law and $\mu$-Law Characteristics

- Create a vector with say 1000 points that spans from −1 to 1.
- Apply A-Law companding on this vector get another vector. Plot it against the first vector for different A values and appreciate the transfer characteristics.
- Repeat the above steps for $\mu$-law as well.

## 2 Practical A-Law compander

- Implement the 8-bit practical A-law coder and decoder in Appendix B 2 (pp 583–585) in *Digital Telephony by Bellamy*
- Test it with random numbers and speech signals. Observe the 15 levels of quantization.

## 3 Practical $\mu$-Law compander

- Implement the 8-bit practical $\mu$-law coder and decoder in Appendix B 1 (pp 579–581) in *Digital Telephony by Bellamy*
- Test it with random numbers and speech signals. Observe the 15 levels of quantization.

## 4 BPSK Transmitter and Receiver

- Cretae a random binary sequence of 5000 bit. Convert it into a bipolar NRZ code.
- Create a BPSK mapper that maps bit 0 to zero phase and bit 1 to $\pi$ phase.
- Plot the real part of the mapped signal against the imaginary part to observe the signal constellation
- Add AWGN of difference variances to the base band BPSK signal and observe the changes in constellation.
- Realize the BPSK transmitter and receiver in Fig. 6.4 in pager 352 in

*Communication Systems by Simon Haykin* .

- Add AWGN of different variances and compute the bit error rate (BER) for different SNR values.
- Plot the BER Vs. SNR.
- Plot the theoretical BER-SNR curve, using Eq. 6.19 in pager 351 in *Communication Systems by Simon Haykin* .

## 5 QPSK Transmitter and Receiver

- Create a random binary sequence of 5000 bit. Convert it into a bipolar NRZ code.
- Create a QPSK mapper that maps bit patterns 00, 10, 11 and 01 to suitable phase values that are odd multiples of $\pi$ .4←
- Plot the real part of the mapped signal against the imaginary part to observe the signal constellation
- Add AWGN of difference variances to the base band QPSK signal and observe the changes in constellation.
- Realize the QPSK transmitter and receiver in Fig. 6.8 in page 359 in *Communication Systems by Simon Haykin* .
- Add AWGN of different variances and compute the bit error rate (BER) for different SNR values.
- Plot the BER Vs. SNR.
- Plot the theoretical BER-SNR curve, using Eq. 6.33 in page 358 in *Communication Systems by Simon Haykin* .

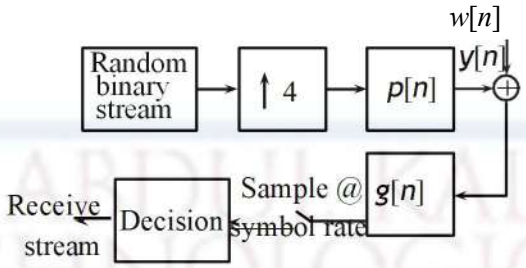
## 6 Matched Filter Receiver

The task is to develop a matched filter receiver, with zero ISI, as shown in the figure below.

- Generate 5000 random bits and up sample the stream by 4.
- For zero ISI, the impulse reponse of the transmitter and receiver filters are the RRC pulse with $\alpha = 0.2$.

$$p(t) = g(t) = \left(\frac{4\alpha}{\pi\sqrt{T}}\right)\left[\frac{\cos(1+\alpha)\frac{\pi t}{T} + \frac{T}{4\alpha t}\sin(1-\alpha)\frac{\pi t}{T}}{1-\left(\frac{4\alpha t}{T}\right)^2}\right] \qquad (1)$$

- Plot $p(t)$ and its approximate spectrum and appreciate.




- Add AWGN ($w[n]$) of different variances and compute the BER-SNR curve for the bit patterns received.

| ECT332 | DATA ANALYSIS | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PEC | 2 | 1 | 0 | 3 |

**Preamble:** This course aims to set the foundation for students to develop new-age skills pertaining to analysis of large-scale data using modern tools.

**Prerequisite**: None

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO 1** | Read and write data to and fro spreadsheets and databases |
| **CO 2** | Work with large data as pandas data frames |
| **CO 3** | Perform PCA and cluster analysis on data frames |
| **CO 4** | Perform Bayesian analysis on data frames. |
| **CO 5** | Apply machine learning in data analysis problems |
| **CO 6** | Apply methods in high performance computing for data analysis |

**Mapping of course outcomes with program outcomes**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO 1** | 3 | 3 | | | 3 | | | | | | | 2 |
| **CO 2** | 3 | 3 | 2 | 3 | 3 | | | | | | | |
| **CO 3** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |
| **CO 4** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |
| **CO 5** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |
| **CO 6** | 3 | 3 | 2 | 3 | 3 | 2 | | | | | | 2 |

**Assessment Pattern**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|
| | 1 | 2 | |
| Remember | 10 | 10 | 20 |
| Understand | 30 | 30 | 60 |
| Apply | 10 | 10 | 20 |
| Analyse | | | |
| Evaluate | | | |
| Create | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

| | |
|---|---|
| Attendance | : 10 marks |
| Continuous Assessment Test (2 numbers) | : 25 marks |
| Assignment/Quiz/Course project | : 15 marks |

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1): Read and write data to and fro spreadsheets and databases**

1. Write Python code to read an .xls file using xlrd module. Sve it as a different .xlsx file using openpyxl.
2. Write Python code to read mongodb data base.

**Course Outcome 2 (CO2): Work with pandas dataframes**

1. Write Python code read a table in a pdf file as a pandas dataframe.
2. Write Python code to create a pandas dataframe. Pickle this data and store it. Write another Python code to retrive the data from the pickle.

**Course Outcome 3 (CO3): PCA and Cluster Analysis**

1. Write Python code to perform PCA on a pandas dataframe. Write code to create a scree plot.
2. Write Python code to do K-means clustering.

**Course Outcome 4 (CO4): Bayesian Analysis on Dataframes**

1. Write Python code to compute the posterior probability of a data set with Pymc3
2. Write a python code to evaluate the statistical correlation between variables in 5X5 random data set.

**Course Outcome 5 (CO5): Machine learning in Data Analysis**

1. Write python code to use Keras for training a CNN
2. Write Python code to read an RGB image and convert to gray scale and write the grayscale image in .jpg format.

**Course Outcome 5 (CO6): High Performance Computing Methods in Data analysis**

1. Write Python code to use numexpr for faster parallel computation
2. Write Python code with Ipython-parallel to perform parallel computing with 4 cores.

## SYLLABUS

**Module 1: Overview of Data Analysis and Python**

Numpy and Scipy Python modules for data analysis. Reading and processing spreadsheets and csv files with Python using xlrd, xlwt and openpyxl. Data visualization with Matplotlib. Two dimensional charts and plots. Scatter plots with matplotlib. Three dimensional visualization using Mayavi module. Reading data from sql and mongodb databases with Python.

**Module 2: Big Data Arrays with Pandas**

Familiarization of the python pandas. Reading and writing pandas dataframes. Reading rows and columns from pandas dataframe. Handling NaN values. Reading and writing .txt, .csv, .pdf, .html and json files with pandas. Merging, concatenating and grouping of data frames. Use of pivot tables. Pickling of data frames in Python.

**Module 3: PCA and Cluster Analysis**

Singular value decomposition of a matrix/array. Eigen values and eigen vectors. Principal component analysis of a data frame. Scree plot. Dimensioanality reduction with PCA. Loadings for principal components. Case study with Python. Cluster analysis. Hierarchial and K-means clustering. Interpretation of dendrograms.

**Module 4: Statistical Data Analysis**

Hypothesis testing. Bayesian analysis. Meaning of prior, posterior and likelyhood functions. Use of pymc3 module to compute the posterior probability. MAP Estimation. Credible interval, conjugate distributions. Contingency table and chi square test. Kernel density estimation.

**Module 5: Machine Learning**

Supervised and unsupervised learning. Use of scikit-learn. Regression using scikit-learn. Deep learning with convolutional newural networks. Structure of CNN. Use of Keras and Tensorflow. Machine learning with pytorch. Reading and writing images with openCV. Case study of character recognition with MNIST dataset. High performance computing for machine learning. Use of numba, jit and numexpr for faster Python code. Use of Ipython-parallel.

**Text Books and References**


1. "Python Data Analytics", Fabio Nelli, Apress.
2. "Data Analysis from Scratch with Python", Peters Morgan, AI Sciences.
3. "Python for Data Analysis", Wes McKinny, O'Reilly.
4. "Ipython Interactive Computing and Visualization Cookbook", Cyrille Rossant , PACKT Open Source Publishing
5. "Deep Learning with Python", Francois Chollet, Manning

**Course Contents and Lecture Schedule**

| No | Topic | No. of Lectures |
|---|---|---|
| **1** | **Overview of Data Analysis and Python** | |
| 1.1 | Numpy and Scipy Python modules for data analysis. | 2 |
| 1.2 | Reading and processing spreadsheets and csv files with Python using xlrd, xlwt and openpyxl. | 2 |
| 1.3 | Data visualization with Matplotlib. Two dimensional charts and plots. Scatter plots with matplotlib. Three dimensional visualization using Mayavi module. | 2 |
| 1.4 | Reading data from sql and mongodb databases with Python | 2 |
| **2** | **Big Data Arrays with Pandas** | |
| 2.1 | Intro. To Python pandas | 1 |
| 2.2 | Reading and writing of data as pandas dataframes. Separating header, columns row etc and other manipulations | 3 |
| 2.3 | Reading data from different kind of files, Merging, concatenating and grouping of data frames. Use of pivot tables. Pickilng | 3 |
| **3** | **PCA and Cluster Analysis** | |
| 3.1 | Singular value decomposition of a matrix/array. Eigen values and eigen vectors. | 1 |
| 3.2 | PCA,Scree plot. Dimensioanality reduction with PCA. Loadings for principal components. Case study with Python. Cluster analysis. | 3 |
| 3.3 | Cluster analysis, dendrograms | 2 |
| **4** | **Statistical Data Analysis** | |
| 4.1 | Hypothesis testing. Bayesian analysis. Meaning of prior, posterior and likelyhood functions. Use of pymc3 module to compute the posterior probability. | 3 |
| 4.2 | MAP Estimation. Credible interval, conjugate distributions .Contingency table and chi square test. Kernel density estimation. | 3 |
| 4.3 | Contingency table and chi square test. Kernel density estimation. | 3 |
| **5** | **Machine Learning** | |
| 5.1 | Supervised and unsupervised learning. Use of scikit-learn. Regression | 2 |
| | using scikit-learn. | |
| 5.2 | Deep learning with convolutional newural networks. Structure of CNN. | 2 |
| 5.3 | Use of Keras and Tensorflow. Machine learning with pytorch. Case study of character recognition with MNIST dataset. | 3 |
| 5.4 | High performance computing for machine learning. Use of numba, jit and numexpr for faster Python code. Use of Ipython-parallel. | 2 |

**Simulation Assignments**

1. Download the iris data set and read into a pandas data frame. Extract the heaser and replace with a new header. Extract colums and rows. Extract pivot tables. Filter the data based on the labels. Store a pivot table as a pickle and retrieve it.
2. For the same data sert, perform principal component analysis. Observe the scree plot. Identify the principal components. Obtain a low dimensional data, with only the principal components and compute the mean square error between the original data and the approximated one. Compute the loadings for the principal components.
3. For the same data, perform hierarchical and K-means clustering with Python codes. Obtain dendrograms in each case and appreciate the clusters.
4. Download the MNIST letter data set. Construct a CNN network with appropriate layers using Keras and Tensorflow. Train the CNN with the MNIST data set. Appreciate the selection and use of training, test and cross-validation data sets. Save the model and weights and use the model to identify letter images. You may use openCV for reading images.
5. Write a Python script to generate alphanumeric images (26 upper case, 26 lowercase and 10 numbers each 12 point in size) of say 16X16 dimension out of windows .ttf files. Create 62 folders each containg a data set of every alphanumeric character. Create a new CNN with Keras and Tensorflow. Create a cross validation data set by taking 10 images out of every 62 folder. Use 80% of the total data for training and 20% for testing the CNN. Use an HPCC like system to train the model and save the model and weight. Test this model to recognize letter images. You may use openCV for reading images.
6. Repeat assignment 4 using pytorch instead of Keras
7. Repeat assignment 5 using pytorch instead of Keras

**Model Question Paper**

A P J Abdul Kalam Technological University

Sixth Semester B Tech Degree Examination

Course: ECT 332 Data Analysis

Time: 3 Hrs Max. Marks: 100

PART A

*Answer All Questions*

| | | | |
|---|---|---|---|
| 1 | Create a two dimensional array of real numbers using numpy. Write Python code to pickle this data. | (3) | $K_3$ |
| 2 | Write Python code to import mayavi module and perform 3-D visualization of $x^2 + y^2 + z^2 = 1$ | (3) | $K_3$ |
| 3 | Write Python code to generate a 5 × 5 pandas data frame of random numbers. Add a header to this dataframe. | (3) | $K_3$ |
| 4 | Write Python code to concatenate two dataframes of same num- ber of columns. | (3) | $K_3$ |
| 5 | Write the expression for the singular value decomposition of a matrix $A$ | (3) | $K_3$ |
| 6 | Explain how principal components are isolated using scree plot. | (3) | $K_1$ |
| 7 | State Bayes theorem and explain the significance of the terms prior, likelyhood and posterior. | (3) | $K_1$ |
| 8 | Write Python code with pymc3 to realize a Bernoulli trial with $p(head) = 0.2$ | (3) | $K_3$ |
| 9 | Give the structure a convolutional neural network | (3) | $K_1$ |
| 10 | Compare supervised and unsupervised learning | (3) | $K_1$ |

PART B

*Answer one question from each module. Each question carries 14 mark.*

Module I

| | | | |
|---|---|---|---|
| 11(A) | Write Python code to read a spreadsheet in .xls format a text file in .csv format and put these data into numpy arrays. in both cases, plot the second column against the first column using matplotlib | (8) | $K_3$ |
| 11(B) | Write Python code to read tables from sql and mongodb databases. | (6) | $K_3$ |

OR

| | | | |
|---|---|---|---|
| 12(A) | Write Python code to create a normally distributed 5 × 5 random array and convert it into a matrix. Write code to | (8) | $K_3$ |

compute its inverse and transpose.

| | | | |
|---|---|---|---|
| 12(B) | Write code to read files in .xlsx format using openpyxl | (6) | $K_3$ |

Module II

| | | | |
|---|---|---|---|
| 13(A) | Write Python code to import a table in .xls format into a data frame. Remove all NaN values. | (6) | $K_3$ |
| 13(B) | Write Python code to generate 10 data frames of size 5 × 5 of random numbers and use a *for loop* to concatenate them. Pickle the concatenated dataframe and store it. Write another code to retrieve the dataframe from the pickle. | (8) | $K_3$ |

OR

| | | | |
|---|---|---|---|
| 14(A) | Write Python code to read in a table from a pdf file into a pandas dataframe. Write code to remove the first two columns and write the rest of the dataframe as a json file. | (8) | $K_3$ |
| 14(B) | Explain the term pivot table. Create a pivot table from the above dataframe | (6) | $K_3$ |

Module III

| | | | |
|---|---|---|---|
| 15 | Write Python code to read in table in .xls format, perform PCA analysis on it and produce the scree plot and loadings for the principal components. | (14) | $K_3$ |

OR

| | | | |
|---|---|---|---|
| 16. | Write Python code to perform hierarchial cluster analysis on a pandas dataframe. Explain how dendrograms can be used to classify data. | (14) | $K_3$ |

Module IV

| | | | |
|---|---|---|---|
| 17(A) | Assume that you have a dataset with 57 data points of Gaussian distribution with a mean of 4 and standard deviation of 0.5. Using PyMC3, write Python code to compute:<br>• The posterior distribution<br>• The prior distribution<br>• The posterior predictive distribution | (8) | $K_3$ |

.

| | | | |
|---|---|---|---|
| 17(B) | Write a python code to find the Bayesian credible interval in the above question. How is it different from confidence interval. | (6) | $K_3$ |

OR

| | | | |
|---|---|---|---|
| 18(A) | Write a python code to evaluate the statistical correlation between variables in 10 × 10 random data set. | (8) | $K_3$ |
| 18(B) | Compute the conjugate of the logarithmic function $f(x) = lnx,\ x > 0.$ | (6) | $K_3$ |

Module V

| | | | |
|---|---|---|---|
| 19(A) | Explain the use of numba and numexpr in fatser Python execution with examples | (8) | $K_3$ |
| 19(B) | Explain the use of Keras as a frontend for Tensorflow with Python codes | (6) | $K_3$ |

OR

| | | | |
|---|---|---|---|
| 20(A) | Explain the use of Ipython-parallel in parallel execution of Python code with examples. | (8) | $K_3$ |
| 20(B) | Explain with Python codes how openCV is used to read and writte images. | (8) | $K_3$ |

| ECT352 | DIGITAL IMAGE PROCESSING | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PEC | 2 | 1 | 0 | 3 |

**Preamble:** This course aims to develop the skills for methods of various transformation and analysis of image enhancement, image reconstruction, image compression, image segmentation and image representation.

**Prerequisite**: EVT 306 Digital Signal Processing

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO 1** | Distinguish / Analyse the various concepts and mathematical transforms necessary for image processing |
| **CO 2** | Differentiate and interpret the various image enhancement techniques |
| **CO 3** | Illustrate image segmentation algorithm |
| **CO 4** | Understand the basic image compression techniques |

**Mapping of course outcomes with program outcomes**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO 1** | 3 | 3 | 2 | | 1 | | | | | | | 2 |
| **CO 2** | 3 | 3 | 2 | | 1 | | | | | | | 2 |
| **CO 3** | 3 | 3 | 3 | | 1 | | | | | | | 2 |
| **CO 4** | 3 | 3 | 3 | | 1 | | | | | | | 2 |

**Assessment Pattern**

| Bloom's Category | | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|---|
| | | 1 | 2 | |
| Remember | K1 | 10 | 10 | 10 |
| Understand | K2 | 20 | 20 | 20 |
| Apply | K3 | 20 | 20 | 70 |
| Analyse | K4 | | | |
| Evaluate | | | | |
| Create | | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**
Attendance: 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks. The questions must have 50% representation from theory, and 50% representation from logical/numerical/derivation/ proof.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1):** Analyze the various concepts and restoration techniques for image processing

1. For the given image check whether pixel P and Q have 8 connectivity.
2. Find filtered image using median filter.
3. Explain Weiner filtering.

**Course Outcome 2 (CO2):** Differentiate and interpret the various image enhancement techniques

1. Classify different image enhancement process. Differentiate between spatial domain and frequency domain techniques of image enhancement.
2. What is histogram equalisation? Briefly discuss the underlying logic behind histogram equalisation.
3. Apply mean and median filters over a given image.

**Course Outcome 3 (CO3):** Illustrate image segmentation algorithm

1. Name two basic approaches of image segmentation and mention their differences.
2. How can you decide optimal thresholds when the image contains a background and several foreground objects? Write down a corresponding algorithm.
3. Write down the region growing algorithm. What are its advantages and disadvantages?

**Course Outcome 4 (CO4):** Analyze basic image compression techniques

1. What do you mean by compression ratio? Do you consider that lower compression ratio ensures better images upon reproduction?
2. How can achievable compression ratio to be determined from image histogram?
3. Mention the steps of lossy and lossless JPEG compression

## SYLLABUS

### Module 1

**Digital Image Fundamentals:** Image representation, basic relationship between pixels, elements of DIP system, elements of visual perception-simple image formation model. Vidicon and Digital Camera working principles Brightness, contrast, hue, saturation, mach band effect
**Colour image fundamentals**-RGB, CMY, HIS models, 2D sampling, quantization.

### Module 2

**Review of matrix theory**: row and column ordering- Toeplitz, Circulant and block matrix
**2D Image transforms:** DFT, its properties, Walsh transform, Hadamard transform, Haar transform, DCT, KL transform and Singular Value Decomposition.
**Image Compression:** Need for compression, Basics of lossless compression – bit plane coding, run length encoding and predictive coding, Basics of lossy compression – uniform and non-uniform quantization techniques used in image compression, Concept of transform coding, JPEG Image compression standard.

### Module 3

**Image Enhancement:** Spatial domain methods: point processing- intensity transformations, histogram processing, image subtraction, image averaging. Spatial filtering- smoothing filters, sharpening filters.
Frequency domain methods: low pass filtering, high pass filtering, homomorphic filter

### Module 4

**Image Restoration:** Degradation model, Unconstraint restoration- Lagrange multiplier and constraint restoration
Inverse filtering- removal of blur caused by uniform linear motion, Weiner filtering,
Geometric transformations-spatial transformations

### Module 5

**Image segmentation**: Classification of Image segmentation techniques, region approach, clustering techniques. Segmentation based on thresholding, edge based segmentation. Classification of edges, edge detection, Hough transform, active contour.

### Text Books

1. Gonzalez Rafel C, Digital Image Processing, Pearson Education, 2009
2. S Jayaraman, S Esakkirajan, T Veerakumar, Digital image processing, Tata Mc Graw Hill, 2015

### Reference Books

1. Jain Anil K , Fundamentals of digital image processing: , PHI,1988
2. Kenneth R Castleman , Digital image processing:, Pearson Education,2/e,2003
3. Pratt William K , Digital Image Processing: , John Wiley,4/e,2007

**Course Contents and Lecture Schedule**

| No. | Topic | No. of Lectures |
|---|---|---|
| **1** | **Digital Image Fundamentals** | |
| 1.1 | Image representation, basic relationship between pixels, elements of DIP system, elements of visual perception-simple image formation model | 3 |
| 1.2 | Vidicon and Digital Camera working principles | 1 |
| 1.3 | Brightness, contrast, hue, saturation, mach band effect | 1 |
| 1.4 | **Colour image fundamentals**-RGB, CMY, HIS models | 1 |
| 1.5 | 2D sampling, quantization. | 1 |
| **2** | **Review of matrix theory** | |
| 2.1 | Row and column ordering- Toeplitz, Circulant and block matrix | 2 |
| 2.2 | **2D Image transforms** : DFT, its properties, Walsh transform, Hadamard transform, Haar transform | 3 |
| 2.3 | DCT, KL transform and Singular Value Decomposition. | 3 |
| 2.4 | **Image Compression:** Need for compression, Basics of lossless compression – bit plane coding, run length encoding and predictive coding, Basics of lossy compression – uniform and non-uniform quantization techniques used in image compression, Concept of transform coding, JPEG Image compression standard.. | 2 |
| **3** | **Image Enhancement** | |
| 3.1 | Spatial domain methods: point processing- intensity transformations, histogram processing, image subtraction, image averaging | 2 |
| 3.2 | Spatial filtering- smoothing filters, sharpening filters | 1 |
| 3.3 | Frequency domain methods: low pass filtering, high pass filtering, homomorphic filter. | 2 |
| 4 | **Image Restoration** | |
| 4.1 | Degradation model, Unconstraint restoration- Lagrange multiplier and constraint restoration | 2 |
| 4.2 | Inverse filtering- removal of blur caused by uniform linear motion, Weiner filtering | 2 |
| 4.3 | Geometric transformations-spatial transformations | 2 |
| **5** | **Image segmentation** | |
| 5.1 | Classification of Image segmentation techniques, region approach, clustering techniques | 2 |
| 5.2 | Segmentation based on Thresholding, edge based segmentation | 2 |
| 5.3 | Classification of edges, edge detection, Hough transform, active contour | 3 |

**Simulation Assignments**

The following simulations be done in Scilab/ Matlab/ LabView:

1. Read Image data into the workspace.
2. Determine various transforms using matlab functions.
3. Detect and measure circular objects in an image.
4. Adjust the contrast of the given image.
5. Filter images using predefined filter.
6. Create degraded images affected by motion blur and noise by simulating the models for both. Apply inverse filtering and Weiner filtering methods to the simulated images and compare their performance.
7. Detect an object against the background using various edge detection algorithms and compare their performance.
8. Create a histogram for a gray scale image.
9. Create image at various compression level.
10. Use texture segmentation to identify region based on their texture.

**Model Question paper**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

SIXTH SEMESTER B.TECH DEGREE EXAMINATION, (**Model Question Paper)**

**Course Code: ECT352**

**Course Name: DIGITAL IMAGE PROCESSING**

Max. Marks: 100 Duration: 3 Hours

**PART A**

Answer all questions, each carries 3 marks.

1. Give mathematical representation of digital images? Write down the names of different formats used. K2
2. Explain mach band effect. K2
3. What is SVD? Explain its applications in digital image processing. K3
4. Write the similarity and difference between Hadamard and Walsh transforms K3
5. What are the advantages and disadvantages of block processing K2
6. Name the role of point operators in image enhancement K2
7. What is median filter? Explain the operation in 2D noise image with salt and pepper noise K3
8. Distinguish between linear and nonlinear image restoration. K3
9. Mention the use of derivative operation in edge detection. K4
10. The Pewitt edge operator is much better than Robert operator. Why? Give the matrix. K3

**PART B**

**Answer any one full questions, from each module carries14marks.**

Module 1

1. a) State and explain the 2D sampling theorem. Explain how aliasing errors can be eliminated? (7 marks)

   b) Define the terms brightness, contrast, hue and saturation with respect to a digital image. Explain the terms False contouring and Machband effect. (K1 – CO1) (7 marks)

OR

2. a) Explain elements of visual perception simple image formation model in detail (K1 – CO1) (8 marks)

   b) Explain various color image models and its transformations (K1 - CO1) (6 marks)

Module 2

3. a) Explain the difference between DST and DCT. (K2 - CO1) (4 marks)

   b) Compute the 2D DFT of the 4x4 gray scale image given below. (K3-CO1) (10 marks)

$$f(x,y)=\begin{bmatrix}1&1&1&1\\1&1&1&1\\1&1&1&1\\1&1&1&1\end{bmatrix}.$$

OR

4. a) Construct a Harr transform matrix for N=4. (4 marks) (K3-CO1)

   b) Compute the 8-point DCT for following date X={2,4,6,8,10,6,4,2}. (10 marks)

Module 3

5. a) List histogram image enhancement techniques? Explain each one in detail. (10 marks) K2-CO2

   b) Write a note on color image enhancement. (K2-CO2) (4 marks)

OR

6. a) Describe the following in detail (i) Histogram equalization (ii) LPF and HPF in image enhancement (iii) high boost filters (10 marks)

Module 4

7. a) Assume 4x4 image and filter the image using median filter of 3x3 neighbourhood. Use replicate padding. (K3—CO1) (8 marks)

   b) Explain the digital image restoration. (K1—CO1) (6 marks)

OR

8. a) Explain inverse filtering with necessary equations. (K1-CO1) (6 marks)

   b) Differentiate various noise models. (K2-CO1) (8 marks)

Module 5

9. a) Explain the active contour algorithm for image segmentation any four geometric transformations on an image. (K2-CO3) (7 marks)

   c) Assume 4x4 image and filter the image using median filter of 3x3 neighbourhoods. Use replicate padding (K3—CO1) (7 marks)

OR

10. a) Explain global, adaptive and histogram based thresholding in detail. (7 marks)
    c) Explain Hough transform in detail (7 marks)

| ECT362 | INTRODUCTION TO MEMS | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PEC | 2 | 1 | 0 | 3 |

**Preamble:** This course introduces students to the rapidly emerging, multi-disciplinary, and exciting field of Micro Electro Mechanical Systems.

**Prerequisite**: EST130-Basics of Electrical and Electronics Engineering, EST 100-Engineering Mechanics

**Course Outcomes**

| | |
|---|---|
| CO1 | Describe the working principles of micro sensors and actuators |
| CO2 | Identify commonly used mechanical structures in MEMS |
| CO3 | Explain the application of scaling laws in the design of micro systems |
| CO4 | Identify the typical materials used for fabrication of micro systems |
| CO5 | Explain the principles of standard micro fabrication techniques |
| CO6 | Describe the challenges in the design and fabrication of Micro systems |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | 3 | | | | | | | | | | |
| CO2 | 3 | 3 | | | | | | | | | | |
| CO3 | 3 | 3 | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | |
| CO5 | 3 | 3 | | | | | | | | | | |
| CO6 | 3 | 3 | | | | | | | | | | |

**Assessment Pattern**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|
| | 1 | 2 | |
| Remember | 10 | 10 | 20 |
| Understand | 30 | 30 | 60 |
| Apply | 10 | 10 | 20 |
| Analyse | | | |
| Evaluate | | | |
| Create | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

| | |
|---|---|
| Attendance | : 10 marks |
| Continuous Assessment Test (2 numbers) | : 25 marks |
| Assignment/Quiz/Course project | : 15 marks |

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1):Describe the working principles of micro sensors and actuators**

1. Explain the principle of operation of two types of micro-accelerometers
2. Explain with relevant examples how the principle of electrostatics may be used for the design of MEMS based sensors and actuators.
3. Explain how smart materials can be used for the design of MEMS based sensors and actuators.

**Course Outcome 2 (CO2): Identify commonly used mechanical structures in MEMS**

1. Explain the purpose of micro cantilevers in MEMS systems. What is the relevance of spring constant (k) of a mechanical structure in micro system design?
2. Derive the expression for the magnitude of applied bending moment with reference to pure bending of longitudinal beams.
3. Explain how plates and diaphragms can be used for the design

**Course Outcome 3(CO3): Explain the application of scaling laws in the design of micro systems**

1. Explain force scaling vector, what information does it provide to a MEMS designer?
2. Derive equations for acceleration a, time t and power density P/V based on the Trimmer Force Scaling Vector?
3. Explain why electrostatic actuation is preferred over electromagnetic actuation at the micro-scale.

**Course Outcome 4 (CO4): Identify the typical materials used for fabrication of micro systems**

1. State the relevant properties of Silicon Carbide and Silicon Nitride for use in Microsystems.
2. Explain why Silicon evolved as the ideal substrate material for MEMS fabrication.
3. Explain with examples the advantages of use of polymers in micro systems fabrication?

**Course Outcome 5 (CO5): Explain the principles of standard micro fabrication techniques**

1. Explain the steps involved in photolithography. State the chemicals used in each of the stages along with the operating conditions.
2. Explain the criteria for choice of surface or bulk micromachining techniques in the design of micro systems.
3. Explain with block diagram the steps in LIGA process. State two advantages of LIGA process over other micro machining techniques.

**Course Outcome 6 (CO6): Describe the challenges in the design, fabrication and packaging of Micro systems**

1. Explain the challenges involved in the packaging of Microsystems as compared to microelectronic devices
2. Discuss the various fabrication challenges associated with surface micromachining.

## SYLLABUS

### MODULE I

MEMS and Microsystems: Applications – multidisciplinary nature of MEMS – principles and examples of Micro sensors and micro actuators – micro accelerometer –comb drives - Micro grippers – micro motors, micro valves, micro pumps, Shape Memory Alloys.

Actuation and Sensing techniques: Thermal sensors and actuators, Electrostatic sensors and actuators, Piezoelectric sensors and actuators, magnetic actuators

### MODULE II

Review of Mechanical concepts: Stress, Strain, Modulus of Elasticity, yield strength, ultimate strength – General stress strain relations – compliance matrix. Overview of commonly used mechanical structures in MEMS - Beams, Cantilevers, Plates, Diaphragms – Typical applications

Flexural beams: Types of Beams, longitudinal strain under pure bending – Deflection of beams – Spring constant of cantilever – Intrinsic stresses

### MODULE III

Scaling laws in miniaturization - scaling in geometry, scaling in rigid body dynamics, Trimmer force scaling vector, scaling in electrostatic and electromagnetic forces, scaling in electricity and fluidic dynamics, scaling in heat conducting and heat convection.

Materials for MEMS – Silicon – Silicon compounds – Silicon Nitride, Silicon Dioxide, Silicon carbide, Poly Silicon, GaAs , Silicon Piezo resistors. Polymers in MEMS – SU-8, PMMA, PDMS, Langmuir – Blodgett Films.

**MODULE IV**

Micro System fabrication – Photolithography – Ion implantation- Diffusion – Oxidation – Chemical vapour deposition – Etching

Overview of Micro manufacturing – Bulk micro manufacturing, Surface micro machining , LIGA process –Microstereo lithography

**MODULE V**

Micro system Packaging: general considerations in packaging design – Levels of Micro system packaging. Bonding techniques for MEMS: Surface bonding, Anodic bonding, Silicon - on - Insulator, wire bonding, Sealing – Assembly of micro systems.

Overview of MEMS areas : RF MEMS, BioMEMS, MOEMS, NEMS

**Text Books:**

1. Chang Liu, Foundations of MEMS, Pearson 2012

2. Tai-Ran Hsu, MEMS and Microsystems Design and Manufacture, TMH, 2002

**Reference Books:**

1. Chang C Y and Sze S. M., VLSI Technology, McGraw-Hill, New York, 2000

2. Julian W Gardner, Microsensors: Principles and Applications, John Wiley & Sons, 1994

3. Mark Madou, Fundamentals of Micro fabrication, CRC Press, New York, 1997

4. Stephen D. Senturia, Microsystem design, Springer (India), 2006.

5. Thomas B. Jones, Electromechanics and MEMS, Cambridge University Press, 2001

6. Gregory T.A. Kovacs, Micromachined Transducers Sourcebook, McGraw Hill, 1998

**Course Contents and Lecture Schedule**

| No | Topic | No. of Lectures |
|---|---|---|
| 1.1 | Introduction to MEMS and Microsystems | 1 |
| 1.2 | Applications – multidisciplinary nature of MEMS – principles and examples of Micro sensors and micro actuators – micro accelerometer, comb drives - | 1 |
| 1.3 | Micro grippers – micro motors, | 1 |
| 1.4 | micro valves, micro pumps, Shape Memory Alloys. | 1 |
| 1.5 | Actuation and Sensing techniques : Thermal sensors and actuators, | 1 |
| 1.6 | Electrostatic sensors and actuators | 1 |
| 1.7 | Piezoelectric sensors and actuators, | 1 |
| 1.8 | magnetic actuators | 1 |

| | | |
|---|---|---|
| 2.1 | Review of Mechanical concepts: Stress, Strain, Modulus of Elasticity, yield strength, ultimate strength | 1 |
| 2.2 | General stress strain relations – compliance matrix. | 1 |
| 2.3 | Overview of commonly used mechanical structures in MEMS - Beams, Cantilevers, Plates, Diaphragms – Typical applications | 1 |
| 2.4 | Flexural beams: Types of Beams, longitudinal strain under pure bending | 2 |
| 2.5 | Deflection of beams – Spring constant of cantilever, Intrinsic stresses | 1 |
| | | |
| 3.1 | Scaling laws in miniaturization - scaling in geometry, scaling in rigid body dynamics, Trimmer force scaling vector, | 2 |
| 3.2 | scaling in electrostatic and electromagnetic forces | 1 |
| 3.3 | scaling in electricity and fluidic dynamics, | 1 |
| 3.4 | scaling in heat conducting and heat convection | 1 |
| 3.5 | Materials for MEMS – Silicon – Silicon compounds- Silicon Nitride | 1 |
| 3.6 | Silicon Dioxide, Silicon carbide | 1 |
| 3.7 | Poly Silicon, GaAs , Silicon Piezo resistors | 1 |
| 3.8 | Polymers in MEMS – SU-8, PMMA, | 1 |
| 3.9 | PDMS, Langmuir – Blodgett Film | 1 |
| | | |
| 4.1 | Micro System fabrication,Photolithography– Ion implantation | 2 |
| 4.2 | Diffusion, Oxidation | 1 |
| 4.3 | Chemical vapour deposition, Etching | 1 |
| 4.4 | Overview of Micro manufacturing – Bulk micro manufacturing, | 1 |
| 4.5 | Surface micro machining | 1 |
| 4.6 | LIGA process | 1 |
| 4.7 | Microstereo lithography | 1 |
| | | |
| 5.1 | Micro system Packaging: general considerations in packaging design | 1 |
| 5.2 | Levels of Micro system packaging | 1 |
| 5.3 | Bonding techniques for MEMS : Surface bonding , Anodic bonding | 1 |
| 5.4 | Silicon - on - Insulator , wire bonding | 1 |
| 5.5 | Sealing – Assembly of micro systems | 1 |
| 5.6 | Overview of MEMS areas : RF MEMS, BioMEMS, MOEMS, NEMS | I |

**A P J Abdul Kalam Technological University**

Sixth Semester B Tech Degree Examination

**Course: ECT 362 Introduction to MEMS**

**Time: 3 Hrs Max. Marks: 100**

## PART A

*Answer All Questions*

| | | |
|---|---|---|
| 1 | State an example to justify the multidisciplinary nature of MEMS | 3 |
| 2 | State three applications of MEMS devices in the automotive industry | 3 |
| 3 | Define normal stress and strain, how it is different from shear stress and strain | 3 |
| 4 | Determine the stress in the longitudinal direction of a Silicon rod with rectangular cross section is pulled on both ends with a force of 10mN. The dimensions of the rod being 1 mm X 100μm X 50μm. | 3 |
| 5 | Define the Trimmer force scaling vector | 3 |
| 6 | State one application each of PDMS and PMMA in MEMS fabrication | 3 |
| 7 | Discuss the criteria for selecting materials for the masks used in etching | 3 |
| 8 | Define etch stop? State the different methods used to stop etching | 3 |
| 9 | State the various levels of micro system packaging | 3 |
| 10 | State two applications of NEMS | 3 |

## PART B

*Answer one question from each module. Each question carries 14 marks.*

### Module I

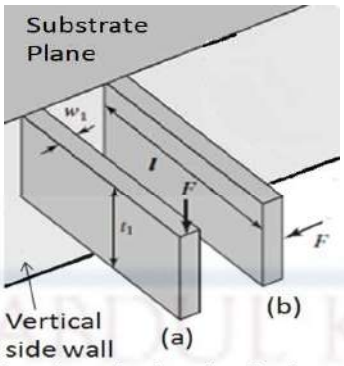
| | | |
|---|---|---|
| 11(A) | Sketch and explain the working of a silicon capacitive accelerometer attached to a comb drive | *6* |
| 11(B) | Explain the operating principle of piezoelectric sensors and actuators with relevant sketches. | *8* |

**OR**

| | | |
|---|---|---|
| 12(A) | Explain the operating principle of thermal bimorphs with neat sketches. State any two applications of thermal sensors. | *8* |
| 12(B) | Explain the principle of operation of the following micro sensors (i) Comb drives (ii) Shape Memory Alloys | *6* |

### Module II

| | | |
|---|---|---|
| 13(A) | Determine the force constant associated with the two beams (a) and (b) shown in figure below.Which is stiffer, justify with arguments. | *8* |




| | | |
|---|---|---|
| 13(B) | Explain with neat sketches the longitudinal strain experienced by segment of beam (with rectangular cross-section) under pure bending. | *6* |

**OR**

| | | |
|---|---|---|
| 14(A) | Explain the general stress strain relationship and arrive at the compliance matrix | *8* |
| 14(B) | Explain with neat sketches the type of mechanical beams and boundary conditions associated with supports | *6* |

**Module III**

| | | |
|---|---|---|
| 15(A) | Explain in the light of scaling, assuming a 10 times reduction of size of the actuator. Which of the electrostatic and electromagnetic forces are best suited for micro device actuation. | *8* |
| 15(B) | State three relevant properties of Silicon Carbide and Silicon Nitride for use in Microsystems | *6* |

**OR**

| | | |
|---|---|---|
| 16(A) | Explain various scaling laws in miniaturization | *6* |
| 16(B) | State the constraints in pumping fluids in micro channels. What pumping scheme is usually used in micro fluidics, state one example? | *8* |

**Module IV**

| | | |
|---|---|---|
| 17(A) | Explain the steps involved in photolithography. State the chemicals used in each of the stages along with the operating conditions | *6* |
| 17(B) | Compare and contrast various micro manufacturing techniques | *8* |

**OR**

| | | |
|---|---|---|
| 18(A) | Describe the various mechanical problems associated with surface micromachining | *6* |
| 18(B) | Explain the LIGA process associated with MEMS fabrication | *8* |

**Module V**

| | | |
|---|---|---|
| 19(A) | Explain the following bonding techniques with figures a) Silicon-on-Insulator b) Wire bonding | |
| 19(B) | Explain the challenges involved in BioMEMS. List three applications of BioMEMS. | *8* |

**OR**

| | | |
|---|---|---|
| 20(A) | Explain with diagrams any two applications of RFMEMS | *8* |
| 20(B) | Explain the challenges involved in designing packages for micro systems | *6* |

| ECT372 | QUANTUM COMPUTING | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PEC | 2 | 1 | 0 | 3 |

**Preamble:** Quantum computers are not yet built. If such machines become a reality, they will fundamentally change how we perform calculations, and the implications on many applications (including communications and computer security) will be tremendous. This course aims to provide a first introduction to quantum computing with a general understanding of how quantum mechanics can be applied to computational problems. It highlights the paradigm change between conventional computing and quantum computing, and introduce several basic quantum algorithms.

**Prerequisite:** MAT101 Linear Algebra and Calculus

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO 1 K2** | Explain the basic constructs in linear algebra needed to build the concepts of quantum computing |
| **CO 2 K2** | Relate the postulates of quantum mechanics for computation and illustrate/ demonstrate quantum measurement |
| **CO 3 K3** | Identify quantum gates and build quantum circuit model in which most of the quantum algorithms are designed. |
| **CO 4 K4** | Analyse and design quantum algorithms and grasp the advantage they offer over classical counterparts. |

**Mapping of course outcomes with program outcomes**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | | | | | | | | | | 2 |
| **CO2** | 3 | 3 | | | | | | | | | | 2 |
| **CO3** | 3 | 3 | 3 | | | | | | | | | 2 |
| **CO4** | 3 | 3 | 3 | 2 | | | | | | | | 2 |

**Assessment Pattern**

| Bloom's Category | | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|---|
| | | 1 | 2 | |
| Remember | K1 | 10 | 10 | 10 |
| Understand | K2 | 20 | 20 | 20 |
| Apply | K3 | 20 | 10 | 50 |
| Analyse | K4 | | 10 | 20 |
| Evaluate | | | | |
| Create | | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1): Explain the basic constructs in linear algebra needed to build the concepts of quantum computing (K2)**

1. Summarise the basic operators and matrices required for understanding the quantum computing concepts.
2. Find the Eigen values and Eigen vectors of Pauli matrices.
3. Explain spectral decomposition and Spectral theorem. State the spectral theorem for Hermitian operator.
4. Show the matrix representation of the tensor products of the Pauli operators

**Course Outcome 2 (CO2): Relate the postulates of quantum mechanics for computation and illustrate/ demonstrate quantum measurement (K2)**

1. State and explain the postulates of Quantum Mechanics applied to computing.
2. Show the Bloch sphere representation of quantum bits.
3. Find the various states of a given system using state space analysis.
4. Demonstrate the state space representation of composite systems using tensor product.

**Course Outcome 3 (CO3): Identify quantum gates and build quantum circuit model in which most of the quantum algorithms are designed (K3)**

1. Model universal gates using standard quantum gates.
2. Illustrate the implementation of quantum operation using quantum gates.
3. Construct and prove circuit identities.
4. Construct a circuit for implementing controlled U operations
5. Design quantum circuits that implements projective measurement in the computational basis.

**Course Outcome 4 (CO4): Analyse and design quantum algorithms and grasp the advantage they offer over classical counterparts (K4)**

1. Design a circuit that implements Quantum Fourier Transform(QFT) for an n-bit input.
2. Construct the phase estimation algorithm from basic principles and design the circuit for phase estimation using QFT.
3. Interpret phase estimation algorithm for the implementation of order finding and factorisation algorithms.

## SYLLABUS

### Module 1: Basics of Linear Algebra

History and Overview of Quantum Computation and Quantum Information, Linear Algebra Basics, Linear Operators and matrices, The Pauli matrices, Inner Products, Eigen values and Eigen vectors, Hermitian operators and Adjoints, Spectral theorem, Tensor Products.

### Module 2: Basics of Quantum Mechanics

State Space Representation - Bloch Sphere, State Evolution – Unitary transformation, Quantum measurement – Projective measurements, Composite systems - Superposition.

### Module 3: Quantum Gates and Circuits

Quantum gates – Hadamard gate, NOT gate, controlled-NOT gate, Toffoli gate, Realisation of classical gates with quantum gates – Z Gate, Fredkein Gate, Pauli Matrices – Controlled Swap and Controlled U-operations, Circuit Identities

### Module 4: Quantum Measurement

Basic principle of quantum measurement - Principle of deferred measurement, Principle of implicit measurement, Gates with projective measurements, Universal quantum gates, Universality of two level unitary gates.

### Module 5: Algorithms

Quantum Fourier Transform (QFT) – Quantum circuit for QFT, Quantum phase estimation, Modular exponentiation, Order finding and factorisation – Deutsch's algorithm.

### Text Books

1. M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information, Cambridge, UK, Cambridge University Press, 2010.
2. J. Gruska, Quantum Computing, McGraw Hill, 1999.
3. G. Strang, Linear algebra and its applications (4th Edition), Thomson, 2006.

**Reference Books**

1. P. Kaye, R. Laflamme, and M. Mosca. An Introduction to Quantum Computing. Oxford, 2007.
2. Eleanor G. Rieffel, Wolfgang H. Polak, "Quantum Computing: A Gentle Introduction," MIT Press, 2011.
3. Noson Yanofsky and Mirco Mannucci, "Quantum Computing for Computer Scientists", Cambridge University Press, 2008.
4. Abhijith, J., Adedoyin, Adetokunbo, Ambrosiano, John (and 30 others), "Quantum Algorithm Implementations for Beginners" , arXiv:1804.03719, 2020.

**Course Contents and Lecture Schedule**

| No | Topic | No. of Lectures |
|---|---|---|
| **1** | **Basics of Linear Algebra** | |
| 1.1 | History and Overview of Quantum Computation and Quantum Information | 1 |
| 1.2 | Linear Algebra Basics | 1 |
| 1.3 | Linear Operators and matrices | 1 |
| 1.4 | Pauli matrices | 1 |
| 1.5 | Inner Products, Eigen values and Eigen vectors | 1 |
| 1.6 | Hermitian operators and Adjoints, Spectral theorem | 2 |
| 1.7 | Tensor Products | 2 |
| | | |
| **2** | **Basics of Quantum Mechanics** | |
| 2.1 | State Space Representation - Bloch Sphere | 1 |
| 2.2 | State Evolution – Unitary transformation | 2 |
| 2.3 | Quantum measurement – Projective measurements | 2 |
| 2.4 | Composite systems - Superposition | 2 |
| | | |
| **3** | **Quantum Gates and Circuits** | |
| 3.1 | Quantum gates – Hadamard gate, NOT gate, controlled-NOT gate, Toffoli gate | 2 |
| 3.2 | Realisation of classical gates with quantum gates – Z Gtae, Fredkein Gate | 2 |
| 3.3 | Pauli Matrices – Controlled Swap and Controlled U-operations | 2 |
| 3.4 | Circuit Identities | 1 |
| | | |
| **4** | **Quantum Measurement** | |
| 4.1 | Basic principle of quantum measurement - Principle of deferred measurement, Principle of implicit measurement | 1 |
| 4.2 | Gates with projective measurements | 2 |
| 4.3 | Universal quantum gates | 1 |

| | | |
|---|---|---|
| 4.4 | Universality of two level unitary gates | 2 |
| | | |
| **5** | **Algorithms** | |
| 5.1 | Quantum Fourier Transform (QFT) | 1 |
| 5.2 | Quantum circuit for QFT Quantum phase estimation | 2 |
| 5.3 | Modular exponentiation | 1 |
| 5.4 | Order finding and factorisation – Deutsch's algorithm | 2 |
| | | |

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

SIXTH SEMESTER B.TECH DEGREE EXAMINATION, (**Model Question Paper)**

**Course Code: ECT372**

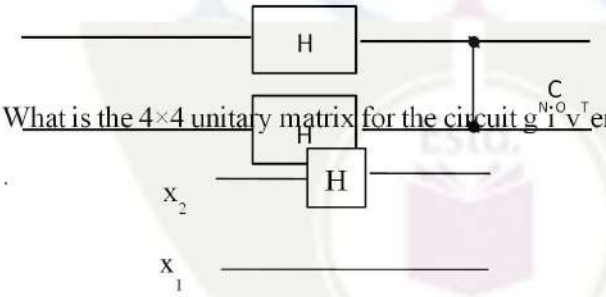
**Course Name: QUANTUM COMPUTING**

Max. Marks: 100 Duration: 3 Hours

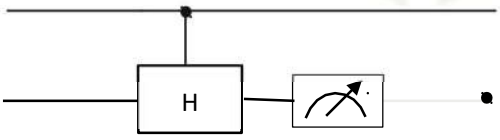
**PART A**

Answer ALL Questions. Each Carries 3 mark.

| | | |
|---|---|---|
| 1 | Consider the operator from $\mathbb{C}^2 \rightarrow \mathbb{C}^2$ given by T(x,y) = (ix, iy), where $\mathbb{Z}^2 = -1$. Find the matrix representation of the Transformation. | K2 |
| 2 | Write the Eigen values and Eigen vectors of the matrix $\begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix}$. Is this operator Hermitian? | K1 |
| 3 | Write down the Bloch sphere representation of the Quantum bit $\frac{1}{2}\|0\rangle + \frac{j}{\sqrt{2}}\|1\rangle$. | K1 |
| 4 | Suppose the first bit of a two bit Quantum System whose state given by $\alpha\|00\rangle + p\|01\rangle + \gamma\|10\rangle + \delta\|11\rangle$ is measured<br>a. What is the probability that the first bit is observed to be 0?<br>b. Suppose that the first bit is observed to be 0, then what is the resultant state of the system? | K3 |
| 5. | Compute the resultant state of the given circuit for input state $\|00\rangle$. | K3 |




| | | |
|---|---|---|
| 6 | What is the 4×4 unitary matrix for the circuit given below | K2 |
| 7 | State the two basic principles of quantum measurement and explain it's uses. | K1 |
| 8 | For the given circuit, 0 was observed by measuring the second bit. What is the resultant Quantum State of the first bit? | K3 |




| | | |
|---|---|---|
| 9 | Give a decomposition of the controlled-Rk gate into single qubit and $C_{NOT}$ gates. | K2 |
| 10 | Draw the 3 input Quantum Fourier Transform (QFT) circuit. | K2 |

## PART – B

## ELECTRONICS & COMMUNICATION ENGINEERING

Answer one question from each module; each question carries 14 marks.

### Module - I

11 a. Find the eigenvectors and eigenvalues of the following four matrices: 7 CO1 K2

$$\sigma_0 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad \sigma_1 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \quad \sigma_2 = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix} \quad \sigma_3 = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$$

b. Give the eigenvalues and eigenvectors of this matrix 7 CO1 K3

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

### OR

12 a. A matrix M is Hermitian if $M^\dagger = M$. Let M be Hermitian. 7 CO1 K3

i. Prove that all of its eigenvalues are real.

ii. Prove that $v^\dagger Mv$ is real, for all vectors v. When $v^\dagger Mv > 0$, we say that $M > 0$.

b. Let M be Hermitian, and define 7 CO1 K3

$$U = e^{iM} = \sum_k \frac{(iM)^k}{k!}$$

Prove that $U^\dagger U = I$, where I is the identity matrix. For matrix M, let $M^\dagger = (M^T)^*$, where $M^T$ is the transpose of M, and * is denotes the complex conjugate of M.

### Module - II

13 a. What is a Quantum State. Explain with examples 2 CO2 K2

b. Consider the following two-qubit quantum state, $|\varphi\rangle$. 12 CO2 K3

$$\frac{\sqrt{2}}{3\sqrt{3}}|00\rangle - \frac{1}{\sqrt{6}}|01\rangle + \frac{2i\sqrt{2}}{3\sqrt{3}}|10\rangle + \frac{5i}{3\sqrt{6}}|11\rangle$$

i. What are the probabilities of outcomes 0 and 1 if the first qubit of $|\varphi\rangle$ is measured?

ii. What are the probabilities of outcomes 0 and 1 if the second qubit of $|\varphi\rangle$ is measured?

iii. What is the state of the system after the first qubit of $|\varphi\rangle$ is measured to be a 0?

iv. What is the state of the system if the second qubit of $|\varphi\rangle$ is measured to be a 1?

v. What are the probabilities of outcomes 0 and 1 if the second qubit of the system is measured, after the first qubit of $|\varphi\rangle$ has been measured to be 0?

vi. What are the probabilities of outcomes 0 and 1 if the first qubit of the system is measured, after the second qubit of $|\varphi\rangle$ has been measured to be 1?

**OR**

14 a. State and explain the four postulates of Quantum Mechanics applied to computing. 8 CO2 K2

b. Which quantum state do we get if we apply (H ⊗ I) CNOT to 6 CO2 K3

$$\sqrt{\frac{1}{3}}|00\rangle + \sqrt{\frac{2}{3}}|11\rangle$$

Here I is the 1-qubit identity operation, H is the 1-qubit Hadamard, and CNOT is the 2-qubit controlled-not operation with the first (=leftmost) qubit being the control.

What is the probability of seeing $|11\rangle$ if we measure the resulting state in the computational basis?

**Module - III**

15 a. Show that XYX = −Y and use this to prove that X $R_y(\theta)$ X = $R_y(-\theta)$. 7 CO3 K3

b. An arbitrary single qubit unitary operator can be written in the form $U = \exp(i\alpha)\, R_{\hat{n}}(\theta)$. for some real numbers α and θ, and a real three-dimensional unit vector $\hat{n}$. 7 CO3 K3

i. Prove this fact.

ii. Find values for α, θ, and $\hat{n}$ giving the Hadamard gate H.

iii. Find values for α, θ, and $\hat{n}$ giving the phase gate.

**OR**

16 a. It is useful to be able to simplify circuits by inspection, using well-known identities. 7

Prove the following three identities:

i. HXH = Z CO3

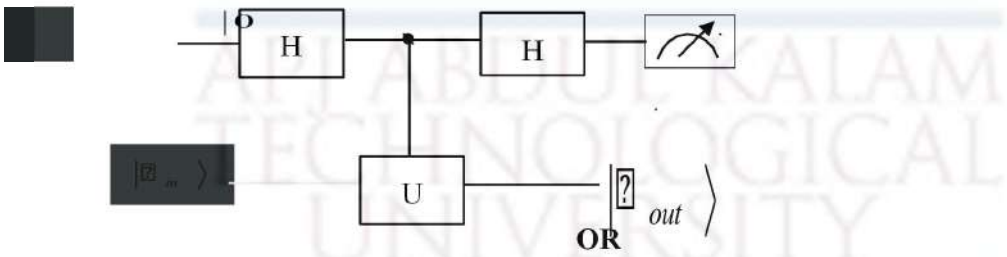
ii. HY H = −Y K3

iii. HZH = X

b. Show that 7 CO3 K3

**Module - IV**

17 Suppose we have a single qubit operator U with eigenvalues ±1, so that U is both Hermitian and unitary. Suppose we wish to measure the observable U. How can this be implemented by a quantum circuit? Show that the following circuit implements a measurement of U. — 14 CO3 K3




**OR**

18 a. Derive the circuit implementing the controlled-U operation for an arbitrary single qubit U, using only single qubit operations and the CNOT gate. — 7 CO3 K4

b. Using just CNOTs and Toffoli gates, construct a quantum circuit to perform the transformation given below. — 7 CO3 K4

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

**Module - V**

19 a. Derive the circuitry for computing a 4-input Quantum Fourier Transform (QFT). — 7 CO4 K3

b. The two qubit Quantum Fourier Transform is given by the following matrix. — 7 CO4 K3

$$F_2 = \frac{1}{2}\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & i & -1 & -i \\ 1 & -1 & 1 & -1 \\ 1 & -i & -1 & i \end{bmatrix}$$

Sketch a circuit for implementing the operator $F_2$ using any combination of 1-qubit Hadamard gates; 1-qubit Pauli gates; 2-qubit CNOT gates and controlled phase shifts. Briefly explain your circuit.

**OR**

| | | | | |
|---|---|---|---|---|
| 20 | a. | Explain the phase estimation algorithm using Quantum Fourier Transform (QFT). Derive the circuitry for the Quantum Phase estimation. | 8 | CO4 K3 |
| | b. | Apply Quantum phase estimation to estimate the phase of a T-Gate. | 6 | CO4 K4 |

| ECT423 | COMPUTER NETWORKS | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PEC | 2 | 1 | 0 | 3 |

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**Preamble:** The course aims to expose students to computer networks taking a top-down approach of viewing from the layer of user applications and zooming into link layer protocols. The principles of various protocols used in every layer are studied in detail. A brief introduction to mathematical modelling of queues with an application to a single example is included.

**Prerequisite:** MAT 204 Probability, Random Process and Numerical Methods

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO1 K2** | Describe the protocols used in web and email applications. |
| **CO2 K4** | Analyse problems pertaining to reliable data transfer, flow control and congestion over a TCP network. |
| **CO3 K3** | Apply Dijkstra's algorithm and distance-vector algorithm in the context of routing over computer networks. |
| **CO4 K4** | Analyze the performance of collision avoidance algorithms in random access protocols such as ALOHA. |
| **CO5 K4** | Analyze the delay performance of an ARQ system using standard queueing models. |

**Mapping of course outcomes with program outcomes**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO 1** | 3 | 3 | 3 | | | | | | | | | 2 |
| **CO 2** | 3 | 3 | 3 | | | | | | | | | 2 |
| **CO 3** | 3 | 3 | 3 | | | | | | | | | 2 |
| **CO 4** | 3 | 3 | 3 | | | | | | | | | 2 |
| **CO 5** | | | | | | | | | | | | |

**Assessment Pattern**

| Bloom's Category | Continuous Assessment Tests | | End Semester Examination |
|---|---|---|---|
| | 1 | 2 | |
| Remember | | | |
| Understand K2 | 10 | 10 | 30 |
| Apply K3 | 20 | 20 | 40 |
| Analyse K4 | 20 | 20 | 30 |
| Evaluate | | | |
| Create | | | |

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 50 | 100 | 3 hours |

**Continuous Internal Evaluation Pattern:**

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

**End Semester Examination Pattern:** There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks. Mark patterns are as per the syllabus with 60 % for theory and 40% for logical/numerical problems, derivation and proof.

**Course Level Assessment Questions**

**Course Outcome 1 (CO1):** Describe the protocols used in web and email applications.

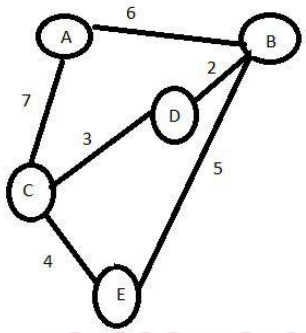
1. Describe the HTTP message format
2. Compare and contrast two application layer protocols SMTP and HTTP

**Course Outcome 2 (CO2:** Analyse problems pertaining to reliale data transfer, flow control and congestion over a TCP network.

1. Why is it that voice and video traffic is often sent over TCP rather than UDP in today's Internet?
2. Suppose two TCP connections are present over some bottleneck link of rate R bps. Both connections have a huge file to send (in the same direction over the bottleneck link). The transmissions of the files start at the same time. What transmission rate would TCP like to give to each of the connections?

**Course Outcome 3 (CO3):** Apply Dijkstra's algorithm and distance-vector algorithm in the context of routing over computer networks.

1. Consider the following network. Compute the shortest-path from the node D to all other nodes using Dijkstra's shortest path algorithm. (Numbers indicated shows the link costs).




2. Consider a router that interconnects three subnets: Subnet 1, Subnet 2, and Subnet 3. Suppose all of the interfaces in each of these three subnets are required to have the prefix 223.1.17/24. Also suppose that Subnet 1 is required to support at least 60 interfaces, Subnet 2 is to support at least 90 interfaces, and Subnet 3 is to support at least 12 interfaces. Provide three network addresses (of the form a.b.c.d/x) that satisfy these constraints.

**Course Outcome 4 (CO4):**Analyze the performance of link-layer protocols in general, random access protocols in particular in terms of efficiency and collision avoidance capability.

1. Describe how slotted ALOHA achieves multiple access.
2. Distinguish between TDM, FDM and random access.

**Course Outcome 5 (CO5):**Analyze the delay performance of an ARQ system using standard queueing models.

1. Consider a network where packets arrive via N different nodes with different arrivate rates. Illustrate the use of Littles law in this scenario to calcualte the average packet delay inside the network.
2. Customers arrive in a restaurant at a rate of 5 per minute, and wait to receive their order for an average of 5 minutes. Customers eat in the restaurant with a probability of 0.5, and carry their order out without eating with probability 0.5. What is the average number of customers in the restaurant?

**SYLLABUS**

| Module | Course contents | Hours |
|---|---|---|
| I | **Components of computer networks** Components of computer network, Applications of computer network – the Internet, Definition of protocol. Protocal standardization.<br><br>**Network edges, Network core and Network links** Client and server hosts, connectionless and connection-oriented services provided to hosts, circuit-switched versus packet-swtiched network cores, FDM, TDM versus statistical multiplexing, Datagram versus Virtual-circuit networks. Access and physical media.<br><br>**Delay and loss in packet-swtiched networks** Types of delay, Packet loss. Layered Architecture: Protocol layering, Internet protocol stack, Message encapsulation.<br><br>**Application Layer** Communication between processes, Web application: HTTP, Mssage format, Email application: SMTP, Message format, MIME, POP3, IMAP and Web-based email. Domain Name System (DNS) | 8 |
| II | **Transport Layer** Multiplexing and demultiplexing: connectionless and connection-oriented. UDP. Procols for reliable data transfer: ARQ protocols, stop-and-wait protocol, alternating-bit protocol, Go-back-N, Selective Repeat.<br><br>**TCP** Connection, segment structure, RTT estimate, Flow control. **Congestion Control** General approaches. TCP congestion control. | 7 |
| III | **Network Layer** Datagram versus virtual-circuit network service, Router architecture, IPv4: datagram format, addressing, address assignement – manual and DHCP, NAT. ICMP. IPv6.<br><br>**Routing Algorithms** Link-State (Dijkstra's) Algorithm, Distance-vector algorithm. Routing in Internet – RIP, OSPF, BGP. Broadcast and Multicast. | 7 |
| IV | **Link Layer** Services of link layer**,** Error detection and corretion – checksum, CRC. Multiple access protocols – Channel partitioning, random access, taking-turns. ALOHA – pure and slotted, efficiency, CSMA, CSMA/CA, CSMA/CD. Link layer addressing: MAC address, ARP, DHCP. Ethernet. Link virtualization: ATM, MPLS | 7 |

| | | |
|---|---|---|
| V | **Wireless Networks** IEEE 802.11 wireless LAN<br><br>**Queueing models in computer networks** Littles theorem and examples. Review of Poisson process. M/G/1 Queue. Delay analysis of Go-Back-N ARQ system. | 8 |

**Text Books**

1. James F. Kurose, Keith W. Ross, Computer Networking: A Top-Down Approach Featuring the Internet, 3rd edition, Pearson
2. D. Bertsekas, RG Gallager, Data Networks, Prentice Hal

**Reference Books**

1. Larry L. Peterson, Bruce S. Davie, Computer Networks – A Systems Approach, Morgan Kauffman
2. N. Abramson, F. Kuo, Computer Communication Networks, Prentice Hall
3. A. S. Tanenbaum, D. J. Wetherall, Computer Networks, Pearson
4. A. Kumar, D. Manjunath, J. Kuri, Communication Networking – An Analytical Approach, Morgan Kauffman Series.

**Course content and Lecture plan**

| No | TOPIC | No of Lectures |
|---|---|---|
| | **MODULE 1** | |
| 1.1 | Components of computer networks, Applications, Protocol, Protocol standrdization | 1 |
| 1.2 | Hosts, connectionless and connection-oriented, circuit-switching versus packet-swtiching in network core design, FDM, TDM versus statistical multiplexing, | 1 |
| 1.3 | Datagram versus Virtual-circuit networks. Examples of access networks, and examples of physical media. | 1 |
| 1.4 | Types of delay, Packet loss. | 1 |
| 1.5 | Layered Architecture, Protocol layering, Internet protocol stack, Message encapsulation. | 1 |
| 1.6 | Communication between processes, HTTP, Mssage format | 1 |
| 1.7 | Email application: SMTP, Message format, MIME, POP3, IMAP and Web-based email. | 1 |
| 1.8 | Domain Name System (DNS) | 1 |
| | **MODULE II** | |
| 2.1 | Services of transport layer, Multiplexing and demultiplexing. Connectionless and connection-oriented transport. UDP. | 1 |
| 2.2 | Procols for reliable data transfer: ARQ protocols, stop-and-wait protocol, alternating-bit protocol, Go-back-N, Selective Repeat. | 3 |

| | | |
|---|---|---|
| 2.3 | TCP Connection, TCP segment, RTT, Flow control. | 1 |
| 2.4 | Congestion, Congestion control. TCP congestion control. | 2 |
| | **MODULE III** | |
| 3.1 | Services of Network Layer,Recap of Datagram versus virtual-circuit network service, Router. | 1 |
| 3.2 | IPv4 addressing, Address assignement – manual and DHCP, NAT. ICMP. IPv6. | 2 |
| 3.3 | Link-State (Dijkstra's) Algorithm, Distance-vector algorithm. | 2 |
| 3.4 | Routing in Internet – RIP, OSPF, BGP. Distinction between Broadcast and Multicast routing. | 2 |
| | **MODULE IV** | |
| 4.1 | Services of link layer**,** Parity checks, checksum, CRC. | 1 |
| 4.2 | Multiple access protocols – Channel partitioning, random access, taking-turns. | 1 |
| 4.3 | ALOHA – pure and slotted, efficiency, CSMA, CSMA/CA, CSMA/CD. | 2 |
| 4.4 | Link layer addressing: MAC address, ARP, DHCP. | 1 |
| 4.5 | Ethernet | 1 |
| 4.6 | Link virtualization: ATM, MPLS | 1 |
| | **MODULE V** | |
| 5.1 | IEEE 802.11 wireless LAN | 1 |
| 5.2 | Mathematical modeling of queues/buffers. | 1 |
| 5.3 | Littles theorem and examples. | 2 |
| 5.4 | Review of Poisson process. M/G/1 Queue | 1 |
| 5.5 | Delay analysis of Go-Back-N ARQ system. | 3 |

**Simulation Assignments**

**Assignment 1:**

1. Understanding protocols using Wireshark.
2. Wireshark is a standard network packet analyzer tool which can be used to analyze how the different protocol layers work (by adding headers and other meta information) to an application layer message.
3. Students can download Wireshark for their OS from https://www.wireshark.org/download.html
4. Sample packet traces can be obtained from https://wiki.wireshark.org/SampleCaptures or https://gitlab.com/wireshark/wireshark/-/wikis/SampleCaptures. Examples such as TCP, DHCP, DNS can be viewed.
5. https://gaia.cs.umass.edu/kurose_ross/wireshark.php

**Assignment 2: (requires Python/Matlab)**

1. Programming/Implementation of Dijsktra's and distance vector algorithm for shortest path on a graph.
2. Representation of networks in a programming language – Sstudents can use NetworkX library in Python for this.
3. Generation of random graphs (students can use inbuilt functions of NetworkX – see for example https://networkx.org/documentation/stable/reference/generators.html)
4. Visualization of the generated graphs can be done using https://networkx.org/documentation/stable/reference/drawing.html
5. Use inbuilt shortest path functions to obtain a baseline to test self-written code https://networkx.org/documentation/stable/reference/algorithms/shortest_paths.html)
6. Implementation of Dijsktra's algorithm (see https://en.wikipedia.org/wiki/Dijkstra%27s_algorithm)
7. Implementation of Bellman Ford's algorithm (https://en.wikipedia.org/wiki/Distance-vector_routing_protocol)
8. Compare your answers with that of the inbuilt functions.
9. Do the assignment following the instructions here: https://media.pearsoncmg.com/aw/aw_kurose_network_3/labs/lab6/lab6.html

**Assignment 3: (understanding TCP)**

1. Fully fledged simulation using NS3 can be given as a demonstration by the instructor https://www.cse.iitb.ac.in/~mythili/teaching/cs224m_autumn2017/tcpsimpa/index.html
2. Do the assignment following the instructions here: https://media.pearsoncmg.com/aw/aw_kurose_network_3/labs/lab5/lab5.html
3. Do the assignment following the instructions here: https://media.pearsoncmg.com/ph/esm/ecs_kurose_compnetwork_8/cw/#interactiveanimations
4. Do the assignment following the instructions here: https://media.pearsoncmg.com/ph/esm/ecs_kurose_compnetwork_8/cw/content/interactiveanimations/tcp-congestion/index.html

**Assignment 4: (basic queueing model and Little's law)**

1. Assignment 4 in the attached collection is a good to understand Littles law. https://drive.google.com/file/d/1CXauy0ehYno1ih6Zwllc_2XFLIe7cH6s/view

2. Do the assignment following the instructions here: https://media.pearsoncmg.com/ph/esm/ecs_kurose_compnetwork_8/cw/content/interactiveanimations/queuing-loss-applet/index.html

**Model Question paper**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

VII SEMESTER B. TECH DEGREE EXAMINATION, (**Model Question Paper)**

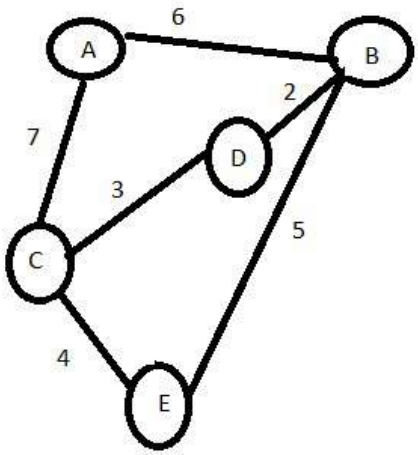
**Course Code: ECT423**

**Course Name: COMPUTER NETWORKS**

Max. Marks: 100 Duration: 3 Hours

| | | |
|---|---|---|
| | **PART A**<br><br>**Answer all questions, each carries3marks** | |
| 1 | Compare and contrast circuit switching and packet switching. | 3 |
| 2 | Explain the concept of FTTH internet access. | 3 |
| 3 | How does the process-to-process delivery service is achieved in transport layer? | 3 |
| 4 | Describe stop-and-wait protocol for reliable data transfer. | 3 |
| 5 | Give the basic blocks in router architecture. | 3 |
| 6 | What are the different error reporting messages in ICMP? | 3 |
| 7 | Explain the frame structure of Ethernet. | 3 |
| 8 | Compare and contrast different random-access protocols. | 3 |
| 9 | Customers arrive in a restaurant at a rate of 5 per minute, and wait to receive their order for an average of 5 minutes. Customers eat in the restaurant with a probability of 0.5, and carry their order out without eating with probability 0.5. What is the average number of customers in the restaurant? | 3 |
| 10 | Define M/G/1 queue. | 3 |
| | **PART B**<br><br>**Answer any one full question from each module carries14marks.** | |
| | **MODULE 1** | |
| 11(a) | How layered architecture helps in the efficient communication between hosts? | 4 |
| 11(b) | Explain the functions performed by the layers in the internet protocol stack. | 10 |
| | **OR** | |

| | | |
|---|---|---|
| 12(a) | Two hosts A and B separated by a distance of *m* meters, connected by a single link of rate *R* bps. The speed of propagation along the link is *s* m/s and host A is to send a packet of size *L* bits to host B.<br>i) Express the propagation delay (□□) in terms of *m* and *s.*<br>ii) Express the transmission delay □□) in terms of *L* and *R.*<br>iii) If *m*=1000meters, $s=2.9 \times 10^8$m/s, *L*=100bits. Find the transmission rate of the link. (Assuming □□ = □□) | 8 |
| 12(b) | Describe any one of the mail access protocols. | 6 |
| | **MODULE II** | |
| 13(a) | Explain how TCP provides a flow control service to its applications. | 5 |
| 13(b) | Compare and contrast TCP and UDP. Also explain the TCP segment structure. | 9 |
| | **OR** | |
| 14(a) | Host A and B are communicating over a TCP connection, and Host B has already received from A all bytes up through byte 248. Suppose Host A then sends two segments to Host B back-to-back. The first and second segments contain 40 and 60 bytes respectively. In the first segment, the sequence number is 249, the source port number is 503, and the destination port number is 80. Host B sends an acknowledgement whenever it receives a segment from Host A.<br>i) In the second segment, sent from Host A to B, what are the sequence number, source port number, and destination port number?<br>ii) If the second segment arrives before the first segment, in the acknowledgement of the first arriving segment. What is the acknowledgement number?<br>iii) If the first segment arrives before the second segment, in the acknowledgement of the first arriving segment, what is the acknowledgement number, the source port number, and the destination port number? | 7 |
| 14(b) | With the help of a neat diagram explain the operation of selective repeat ARQ. | 7 |
| | **MODULE III** | |
| 15(a) | Explain the datagram format in IPv4 | 7 |
| 15(b) | Describe the Internet's address assignment strategy using classless interdomain routing. | 7 |
| | **OR** | |
| 16(a) | Describe the process of assigning IP address to a host in an organization using DHCP protocol. | 5 |
| 16(b) | Consider the following network. Compute the shortest-path from the node D to all other nodes using Dijkstra's shortest path algorithm. (Numbers indicated shows the link costs). | 9 |

| | | |
|---|---|---|
| |  | |
| | **MODULE IV** | |
| 17(a) | Explain the multiple access protocol used in IEEE 802.3. | 7 |
| 17(b) | Explain the error detection mechanism using CRC with an example. | 7 |
| | **OR** | |
| 18(a) | Derive the efficiency of slotted ALOHA. | 7 |
| 18(b) | Explain how the physical address of a host is being mapped from its IP address using address resolution protocol. | 7 |
| | **MODULE V** | |
| 19(a) | State and prove Littles theorem. | 7 |
| 19(b) | Explain the IEEE 802.11 MAC protocol. | 7 |
| | **OR** | |
| 20(a) | Derive an expression for the average packet delay in a Go-Back-N ARQ system. | 7 |
| 20(b) | Describe how a wireless station associates with an access point (AP) as per IEEE 802.11 protocol. | 7 |

| EVL332 | VLSI DESIGN LAB | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PCC | 0 | 0 | 3 | 2 |

1. **Preamble:** This course aims to (i) digital logic gates and their implementation using Verilog ii) Learn the principles of designing and implementing basic combinational and sequential circuits iii) Develop the ability to synthesize complex digital circuits using EDA tools such as FOSS tools, Cadence, and Synopsys.

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**Prerequisite: ECT 203 Logic Circuit Design, EVT 204 Digital System Design**

**Course Outcomes:** After the completion of the course the student will be able to

| | |
|---|---|
| **CO 1** | Develop a fundamental understanding of digital logic gates and their implementation using Verilog. |
| **CO 2** | Learn the principles of designing and implementing basic combinational and sequential circuits. |
| **CO 3** | Gain experience in using synthesis tools to optimize and implement digital circuits. |

**Mapping of course outcomes with program outcomes**

| | PO1 | PO 2 | PO3 | PO 4 | PO5 | PO 6 | PO7 | PO8 | PO9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | | | | | | 2 | | | 2 |
| **CO2** | 3 | 3 | 3 | 2 | 3 | | | | 2 | | | 2 |
| **CO3** | 2 | 2 | 2 | | 2 | | | | 3 | 2 | | 3 |

**Assessment**
**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 75 | 75 | 3 hours |

**Continuous Evaluation Pattern**

Attendance : 15 marks
Continuous Assessment : 30 marks
Internal Test (Immediately before the second series test) : 30 marks

**End Semester Examination Pattern:** The following guidelines should be followed regarding awardof marks

(a) Preliminary work : 15 Marks
(b) Implementing the work/Conducting the experiment : 10 Marks
(c) Performance, result and inference (usage of equipments and trouble shooting): 25 Marks
(d) Viva voce : 20 marks
(e) Record : 5 Marks

**General instructions:** End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

**Course Level Assessment Questions (Examples only)**

**Course Outcome 1 (CO1):** Develop a fundamental understanding of digital logic gates and their implementation using Verilog.

1. Write Verilog codes using gate-level modeling to implement AND, OR, NOT, XOR, and XNOR logic gates. Simulate and verify the output waveforms.
2. Design a 2-bit half adder using **dataflow**, **gate-level**, and **behavioral modeling** in Verilog. Compare the simulation results of all three styles.
3. Construct a 2-bit full adder using two half adders and implement it using structural modeling in Verilog. Explain the interconnection between the modules.

**Course Outcome 2 (CO2):** Learn the principles of designing and implementing basic combinational and sequential circuits.

1. Write behavioral Verilog codes for the following combinational circuits:
   a) 8:1 multiplexer
   b) 1:16 demultiplexer
   c) 16:4 encoder and 3:8 decoder
   Simulate and verify all outputs.
2. Design and simulate the following flip-flops in Verilog using behavioral modeling: SR, D, JK, and T flip-flops. Explain their characteristic equations and timing behavior.
3. Implement a 3-bit magnitude comparator using both behavioral and structural modeling styles in Verilog. Validate functionality through simulation.

**Course Outcome 3 (CO3):** Gain experience in using synthesis tools to optimize and implement digital circuits.

1. Use a synthesis tool (FOSS/Cadence/Synopsys) to synthesize the Verilog codes for basic logic gates (AND, OR, NOT, XOR, XNOR). Analyze and compare area, delay, and power consumption.
2. Synthesize the Verilog implementations of the 2-bit half adder and 2-bit full adder using a synthesis tool. Generate the netlist and examine the gate-level realization.
3. Design a FIFO buffer in Verilog and synthesize it using an EDA tool (FOSS/Cadence/Synopsys). Discuss synthesis results and potential optimizations.

**List of Experiments:**

| |
|---|
| 1. Write Verilog codes to realize the logic gates: AND, OR, NOT, XOR and XNOR |
| 2. Write Verilog codes to realize a 2-bit half adder in all three modeling styles |
| 3. Write a structural Verilog code to realize a 2-bit full adder |
| 4. Write a Verilog code to realize a 2-bit full adder using two half adders |
| 5. Write a behavioural Verilog code to realize a 8:1 MUX |
| 6. Write a behavioural Verilog code to realize a 1:16 DE-MUX |
| 7. Write a behavioural Verilog code to realize a 16:4 encoder |
| 8. Write a behavioural Verilog code to realize a 3:8 decoder |
| 9. Write Verilog codes to realize SR, D, JK and T flip-flops |
| 10. Realize a 3-bit comparator in Verilog using behavioural and structural modeling |
| 11. Realize ring and Johnson counters in Verilog using data-flow modeling |
| 12. Realize a BCD counter in Verilog using gate level abstraction (structural modeling) |
| 13. Synthesize the basic logic gates using FOSS/Cadence/Synopsys tool |
| 14. Synthesize both half adder and full adder using FOSS/Cadence/Synopsys tool |
| 15. Realize a FIFO in Verilog and synthesize using FOSS/Cadence/Synopsys tool |

**Text Books:**

1. Digital Design: With an Introduction to the Verilog HDL, *M. Morris Mano and Michael D. Ciletti,* 5th Edition, Pearson.

2. **Verilog HDL: A Guide to Digital Design and Synthesis,** *Samir Palnitkar,* 2nd Edition, Pearson Education

| ECD334 | MINIPROJECT | CATEGORY | L | T | P | CREDIT |
|---|---|---|---|---|---|---|
| | | PWS | 0 | 0 | 3 | 2 |

**Preamble:** The course aims

- To estimate the ability of the students in transforming the theoretical knowledge studied in to a working model of an electronic system
- For enabling the students to gain experience in organisation and implementation of small projects.
- Design and development of Small electronic project based on hardware or a combination of hardware and software for electronics systems.

**Course Plan**

In this course, each group consisting of three/four members is expected to design and develop a moderately complex electronic system with practical applications, this should be a working model. The basic concept of product design may be taken into consideration.

Students should identify a topic of interest in consultation with Faculty/Advisor. Review the literature and gather information pertaining to the chosen topic. State the objectives and develop a methodology to achieve the objectives. Carryout the design/fabrication or develop codes/programs to achieve the objectives. Demonstrate the novelty of the project through the results and outputs. The progress of the mini project is evaluated based on a minimum of two reviews.

The review committee may be constituted by the Head of the Department. A project report is required at the end of the semester. The product has to be demonstrated for its full design specifications. Innovative design concepts, reliability considerations, aesthetics/ergonomic aspects taken care of in the project shall be given due weight.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Be able to practice acquired knowledge within the selected area of technology for project development. |
| **CO2** | Identify, discuss and justify the technical aspects and design aspects of the project with a systematic approach. |
| **CO3** | Reproduce, improve and refine technical aspects for engineering projects. |
| **CO4** | Work as a team in development of technical projects. |
| **CO5** | Communicate and report effectively project related activities and findings. |

**Mapping of course outcomes with program outcomes**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO 1** | 3 | 3 | 3 | 2 | | 3 | | | | | | 2 |
| **CO 2** | 3 | 3 | 3 | 2 | | 3 | | | | | 3 | 2 |
| **CO 3** | 3 | 3 | 3 | 2 | | 3 | | | | | 3 | 2 |
| **CO 4** | | | | | | | | 3 | | 3 | 3 | 2 |
| **CO 5** | | | | | | | | 3 | 3 | 3 | | 2 |

**Evaluation**

The internal evaluation will be made based on the product, the report and a viva- voce examination, conducted by a 3-member committee appointed by Head of the Department comprising HoD or a senior faculty member, Academic coordinator for that program, project guide/coordinator.

The Committee will be evaluating the level of completion and demonstration of functionality/specifications, presentation, oral examination, work knowledge and involvement.

**Mark distribution**

| Total Marks | CIE | ESE | ESE Duration |
|---|---|---|---|
| 150 | 75 | 75 | 1 hour |

**Split-up of CIE**

| Component | Marks |
|---|---|
| Attendance | 10 |
| Marks awarded based on guide's evaluation | 15 |
| Project Report | 10 |
| Evaluation by Committee | 40 |

**Split-up of ESE**

| Component | Marks |
|---|---|
| Level of completion | 10 |
| Demonstration of functionality | 25 |
| Project Report | 10 |
| Viva-voce | 20 |
| Presentation | 10 |