B TECH IN

ELECTRONICS (VLSI DESIGN & TECHNOLOGY)

SEMESTER 3

SLOT	COURSE NO.	COURSES	L-T-P	HOURS	CREDITS
A	MAT201	PARTIAL DIFFERENTIAL EQUATION AND COMPLEX ANALYSIS	3-1-0	4	4
B	ECT201	SOLID STATE DEVICES	3-1-0	4	4
C	ECT 203	LOGIC CIRCUIT DESIGN	3-1-0	4	4
D	ECT205	NETWORK THEORY	3-1-0	4	4
E 1/2	EST200	DESIGN AND ENGINEERING	2-0-0	2	2
	HUT200	PROFESSIONAL ETHICS	2-0-0	2	2
F	MCN201	SUSTAINABLE ENGINEERING	2-0-0	2	--
S	ECL 201	SCIENTIFIC COMPUTING LAB	0-0-3	3	2
T	ECL 203	LOGIC DESIGN LAB	0-0-3	3	2
R/M	VAC	Remedial/Minor course	3-1-0	4**	4
		TOTAL		26/30	22/26

SEMESTER 4

SLOT	COURSE NO.	COURSES	L-T-P	HOURS	CREDIT
A	MAT 204	PROBABILITY, RANDOM PROCESS AND NUMERICAL METHODS	3-1-0	4	4
B	ECT202	ANALOG CIRCUITS	3-1-0	4	4
C	EVT204	DIGITAL SYSTEM DESIGN	3-1-0	4	4
D	ECT 206	COMPUTER ARCHITECTURE AND MICROCONTROLLERS	3-1-0	4	4
E 1/2	EST200	DESIGN AND ENGINEERING	2-0-0	2	2
	HUT200	PROFESSIONAL ETHICS	2-0-0	2	2
F	MCN202	CONSTITUTION OF INDIA	2-0-0	2	--
S	ECL 202	ANALOG CIRCUITS AND SIMULATION LAB	0-0-3	3	2
T	ECL 204	MICROCONTROLLER LAB	0-0-3	3	2
R/M/H	VAC	Remedial/Minor/Honours	3-1-0	4**	4
		TOTAL		26/30	22/26

SYLLABUS

FOR

BTECH IN ELECTRONICS (VLSI DESIGN & TECHNOLOGY)

THIRD & FOURTH SEMESTERS

SEMESTER - 3

ECT201	SOLID STATE DEVICES	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to understand the physics and working of solid state devices.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO1	Apply Fermi-Dirac Distribution function and Compute carrier concentration at equilibrium and the parameters associated with generation, recombination and Transport mechanism
CO2	Explain drift and diffusion currents in extrinsic semiconductors and Compute current density due to these effects.
CO3	Define the current components and derive the current equation in a pn junction diode And bipolar junction transistor.
CO4	Explain the basic MOS physics and derive the expressions for drain current in linear And saturation regions.
CO5	Discuss scaling of MOSFETs and short channel effects.

Mapping of course outcomes with program outcomes:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO1	3	3										
CO2	3	3										
CO3	3	3										
CO4	3	3										
CO5	3											

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	20
Understand	25	25	50
Apply	15	15	30
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks

Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Compute carrier concentration at equilibrium and the parametersassociated with generation, recombination and transport mechanism

1. Derive the expression for equilibrium electron and hole concentration.
2. Explain the different recombination mechanisms
3. Solve numerical problems related to carrier concentrations at equilibrium, energy band diagrams and excess carrier concentrations in semiconductors.

Course Outcome 2 (CO2) : Compute current density in extrinsic semiconductors in specifiedelectric field and due to concentration gradient.

1. Derive the expression for the current density in a semiconductor in response to the applied electric field.
2. Derive the expression for diffusion current in semiconductors.
3. Show that diffusion length is the average distance a carrier can diffuse before recombining.

Course Outcome 3 (CO3): Define the current components and derive the current equation in a pn junction diode and bipolar junction transistor.

1. Derive ideal diode equation.
2. Derive the expression for minority carrier distribution and terminal currents in a BJT.
3. Solve numerical problems related to PN junction diode and BJT.

Course Outcome 4 (CO4): Explain the basic MOS physics with specific reference on MOSFET characteristics and current derivation.

1. Illustrate the working of a MOS capacitor in the three different regions of operation.

2. Explain the working of MOSFET and derive the expression for drain current.

3. Solve numerical problems related to currents and parameters associated with MOSFETs.

Course Outcome 5 (CO5): Discuss the concepts of scaling and short channel effects of MOSFET.

1. Explain the different MOSFET scaling techniques.

2. Explain the short channel effects associated with reduction in size of MOSFET.

SYLLABUS

MODULE I

Elemental and compound semiconductors, Intrinsic and Extrinsic semiconductors, concept of effective mass, Fermions-Fermi Dirac distribution, Fermi level, Doping & Energy banddiagram, Equilibrium and steady state conditions, Density of states & Effective density of states, Equilibrium concentration of electrons and holes.

Excess carriers in semiconductors: Generation and recombination mechanisms of excess carriers, quasi Fermi levels.

MODULE II

Carrier transport in semiconductors, drift, conductivity and mobility, variation of mobility with temperature and doping, Hall Effect.
Diffusion, Einstein relations, Poisson equations, Continuity equations, Current flow equations, Diffusion length, Gradient of quasi Fermi level

MODULE III

PN junctions : Contact potential, Electrical Field, Potential and Charge distribution at the junction, Biasing and Energy band diagrams, Ideal diode equation.
Metal Semiconductor contacts, Electron affinity and work function, Ohmic and Rectifying Contacts, current voltage characteristics.
Bipolar junction transistor, current components, Transistor action, Base width modulation.

MODULE IV

Ideal MOS capacitor, band diagrams at equilibrium, accumulation, depletion and inversion, threshold voltage, body effect, MOSFET-structure, types, Drain current equation (derive)- linear and saturation region, Drain characteristics, transfer characteristics.

MODULE V

MOSFET scaling – need for scaling, constant voltage scaling and constant field scaling. Sub

threshold conduction in MOS.
Short channel effects- Channel length modulation, Drain Induced Barrier Lowering, Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects.

Non-Planar MOSFETs: Fin FET –Structure, operation and advantages

Text Books

1. Ben G. Streetman and Sanjay Kumar Banerjee, Solid State Electronic Devices, Pearson 6/e, 2010 (Modules I, II and III)

2. Sung Mo Kang, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill,Third Ed., 2002 (Modules IV and V)

Reference Books

1. Neamen, Semiconductor Physics and Devices, McGraw Hill, 4/e, 2012

2. Sze S.M., Semiconductor Devices: Physics and Technology, John Wiley, 3/e, 2005

3. Pierret, Semiconductor Devices Fundamentals, Pearson, 2006

4. Sze S.M., Physics of Semiconductor Devices, John Wiley, 3/e, 2005

5. Achuthan, K N Bhat, Fundamentals of Semiconductor Devices, 1e, McGraw Hill,2015

6. Yannis Tsividis, Operation and Modelling of the MOS Transistor, Oxford University Press.
7. Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits - A Design Perspective, PHI.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**MODULE 1**	
1.1	Elemental and compound semiconductors, Intrinsic and Extrinsic semiconductors, Effective mass	2
1.2	Fermions-Fermi Dirac distribution, Fermi level, Doping & Energy band diagram,	2
1.3	Equilibrium and steady state conditions, Density of states & Effective density of states	1
1.4	Equilibrium concentration of electrons and holes.	1
1.5	Excess carriers in semiconductors: Generation and recombinationmechanisms of excess carriers, quasi Fermi levels.	2
2	**MODULE 2**	
2.1	Carrier transport in semiconductors, drift, conductivity and mobility, variation of mobility with temperature and doping.	2
2.2	Diffusion equation	1

2.3	Einstein relations, Poisson equations	1
2.4	Poisson equations, Continuity equations, Current flow equations	1
2.5	Diffusion length, Gradient of quasi Fermi level	1
3	**MODULE 3**	
3.1	PN junctions : Contact potential, Electrical Field, Potential and Charge distribution at the junction, Biasing and Energy band diagrams,	2
3.2	Ideal diode equation	1
3.3	Metal Semiconductor contacts, Electron affinity and work function, Ohmic and Rectifying Contacts, current voltage characteristics.	3
3.4	Bipolar junction transistor – working,, current components, Transistoraction, Base width modulation.	2
3.5	Derivation of terminal currents in BJT	2
4	**MODULE 4**	
4.1	Ideal MOS capacitor, band diagrams at equilibrium, accumulation, depletion and inversion	2
4.2	Threshold voltage, body effect	1
4.3	MOSFET-structure, working, types,	2
4.4	Drain current equation (derive)- linear and saturation region, Drain characteristics, transfer characteristics.	2
5	**MODULE 5**	
5.1	MOSFET scaling – need for scaling, constant voltage scaling and constant field scaling.	2
5.2	Sub threshold conduction in MOS.	1
5.3	Short channel effects- Channel length modulation, Drain Induced Barrier Lowering, Velocity Saturation, Threshold Voltage Variations and Hot CarrierEffects.	3
5.4	Non-Planar MOSFETs: Fin FET –Structure, operation and advantages	1

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION,
Course Code :ECT201
Course : SOLID STATE DEVICES

Time: 3 hours **Max. Marks:100**

PART A

Answer ***all*** questions. Each question carries ***3 marks***.

1. Draw the energy band diagram of P type and N type semiconductor materials, clearly indicating the different energy levels.
2. Indirect recombination is a slow process. Justify
3. Explain how mobility of carriers vary with temperature.
4. Show that diffusion length is the average length a carrier moves before recombination.
5. Derive the expression for contact potential in a PN junction diode.
6. Explain Early effect? Mention its effect on terminal currents of a BJT.
7. Derive the expression for threshold voltage of a MOSFET.
8. Explain the transfer characteristics of a MOSFET in linear and saturation regions.
9. Explain Subthreshold conduction in a MOSFET. Write the expression for Subthreshold current.
10. Differentiate between constant voltage scaling and constant field scaling

PART B

Answer ***any one*** question from each module. Each question carries 14 marks.

MODULE I

11. (a) Derive law of mass action (8 marks)

    (b) An n-type Si sample with $N_d = 10^5$ cm^{-3} is steadily illuminated such that $g_{op}=10^{21}$EHP/cm^3 s. If $\tau_n = \tau_p = 1\mu s$ for this excitation. Calculate the separation in the Quasi- Fermi levels (F_n-F_p). Draw the Energy band diagram . (6 marks)

12. (a) Draw and explain Fermi Dirac Distribution function and position of Fermi level in intrinsic and extrinsic semiconductors. (8 marks)

    (b)The Fermi level in a Silicon sample at 300 K is located at 0.3 eV below the bottom of the conduction band. The effective densities of states $N_C = 3.22 \times 10^{19}$ cm^{-3} and $N_V = 1.83 \times 10^{19}$ cm^{-3}. Determine

    (a) the electron and hole concentrations at 300K.

    (b) the intrinsic carrier concentration at 400 K. (6 marks)

MODULE II

13. (a) Derive the expression for mobility, conductivity and Drift current density in a semiconductor. (8 marks)
    (b) A Si bar 0.1 μm long and 100 μm^2 in cross-sectional area is doped with 10^{17} cm^{-3} phosphorus. Find the current at 300 K with 10 V applied. How long will it take an average electron to drift 1 μm in pure Si at an electric field of 100 V/cm? (6 marks)

14. (a) A GaAs sample is doped so that the electron and hole drift current densities are equal in an applied electric field. Calculate the equilibrium concentration of electron and hole, the net doping and the sample resistivity at 300 K. Given μ_n= 8500 cm^2/Vs, μ_p = 400 cm^2/Vs, n_i = 1.79 x 10^6 cm^{-3}. (7 marks)
    (b) Derive the steady-state diffusion equations in semiconductor. (6 marks)

MODULE III

15. (a) Derive the expression for ideal diode equation. State the assumptions use (9 marks)
    (b) Boron is implanted into an n-type Si sample ($N_d = 10^{16} cm^{-3}$), forming an abrupt junction of square cross section with area = 2 x 10^{-3} cm^2 . Assume that the acceptor concentration in the p-type region is N_a = 4 x 10^{18} cm^{-3} . Calculate V_0 , W, Q+, and E_0 for this junction at equilibrium (300 K). (5 marks)

16. With the aid of energy band diagrams, explain how a metal – N type Schottky contact function as rectifying and ohmic contacts. (14 marks)

MODULE IV

17. (a) Starting from the fundamentals, derive the expression for drain current of a MOSFETin the two regions of operation. (8 Marks)
    (b) Find the maximum depletion width, minimum capacitance C_i, and threshold voltagefor an ideal MOS capacitor with a 10-nm gate oxide ($Si0_2$) on p-type Si with $N_a = 10^{16}$ cm^{-3}. Include the effects of flat band voltage, assuming an n + polysilicon gate and fixed oxide charge of 5 x 10^{10} q (C/cm^2). (6 marks)

18. (a) Explain the CV characteristics of an ideal MOS capacitor (8 Marks)
    (b) For a long channel n-MOSFET with W = 1V, calculate the V_G required for an $I_{D(sat.)}$ of 0.1 mA and $V_{D(sat.)}$ of 5V. Calculate the small-signal output conductance g and V the transconductance $g_{m(sat.)}$ at V_D = 10V. Recalculate the new I_D for (V_G - V_T) = 3 and V_D = 4V. (6 marks)

MODULE V

19. Explain Drain induced barrier lowering, Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects associated with scaling down of MOSFETs. (14 marks)
20. With the aid of suitable diagrams explain the structure and working of a FINFET. List its advantages. (14 marks)

ECT203	LOGIC CIRCUIT DESIGN	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to impart the basic knowledge of logic circuits and enablestudents to apply it to design a digital system.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO1	Explain the elements of digital system abstractions such as digital representations of information, digital logic and Boolean algebra
CO2	Create an implementation of a combinational logic function described by a truth table using and/or/inv gates/ muxes
CO3	Compare different types of logic families with respect to performance and efficiency
CO4	Design a sequential logic circuit using the basic building blocks like flip-flops
CO5	Design and analyze combinational and sequential logic circuits through gate level Verilog models.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO1	3	3										
CO2	3	3	3									
CO3	3	3										
CO4	3	3	3									
CO5	3	3	3									

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	20
Understand	25	25	50
Apply	15	15	30
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks

Course project : 15 marks

It is mandatory that a *course project* shall be undertaken by a student for this subject. The course project can be performed either as a hardware realization/simulation of a typical digital system using combinational or sequential logic. Instead of two assignments, two evaluations may be performed on the course project along with series tests, each carrying 5 marks. Upon successful completion of the project, a brief report shall be submitted by the student which shall be evaluated for 5 marks. The report has to be submitted for academic auditing. A few samples projects are given below:

Sample course projects:

1. M-Sequence Generator Psuedo random sequences are popularly used in wireless communication. A sequence generator is used to produce pseudo random codes that are useful in spread spectrum applications. Their generation relies on irreducible polynomials.A maximallength sequence generator that relies on the polynomial P (D) = $D^7 + D^3 + 1$, with each D represent delay of one clock cycle.

- An 8-bit shift register that is configured as a ring counter may be used realize the aboveequation.
- This circuit can be developed in verilog, simulated, synthesized and programmed into a tinyFPGA and tested in real time.
- Observe the M-sequnce from parallel outputs of shift register for one period . Count thenumber of 1s and zeros in one cycle.
- Count the number of runs of 1s in singles, pairs, quads etc. in the pattern.

2. BCD Subtractor

- Make 4 -bit parallel adder circuit in verilog.
- Make a one digit BCD subtracter in Verilog, synthesize and write into a tiny FPGA.
- Test the circuit with BCD inputs.

3. Digital Thermometer

- Develop a circuit with a temperature sensor and discrete components to measure and dispaly temperature.
- Solder the circuit on PCB and test it.

4. Electronic Display

- This display should receive the input from an alphanumeric keyboard and display it on an LCD diplay.
- The decoder and digital circuitry is to developed in Verilog and programmed into a tiny FPGA.

5. Electronic Roulette Wheel

- 32 LEDs are placed in a circle and numbered that resembles a roulette wheel.
- A 32-bit shift register generates a random bit pattern with a single 1 in it.

- When a push button is pressed the single 1 lights one LED randomly.
- Develop the shift register random pattern generator in verilog and implement on a tiny FPGA and test the circuit.

6. **Three Bit Carry Look Ahead Adder**
   - Design the circuit of a three bit carry look ahead adder.
   - Develop the verilog code for it and implement and test it on a tiny FPGA. Compare the performance with a parallel adder.

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks. The questions on verlog modelling should not have a credit more than 25% of the whole mark

Course Level Assessment Questions

Course Outcome 1 (CO1) : Number Systems and Codes

1. Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2‘s complement form. Find the value of the following mathematical expression (i) A + B(ii)A – B
2. Perform the following operations (i)$D9CE_{16}$-$CFDA_{16}$ (ii) 6575_8-5732_8
3. Convert decimal 6,514 to both BCD and ASCII codes. For ASCII, an even parity bit is tobe appended at the left.

Course Outcome 2 (CO2) : Boolean Postulates and combinational circuits

1. Design a magnitude comparator to compare two 2-bit numbers A = A_1A_0 and B = B_1B_0B2. Simplify using K-map F(a,b,c,d) = Σ m (4,5,7,8,9,11,12,13,15)
2. Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = Σ m (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)

Course Outcome 3 (CO3) : Logic families and its characteristics

1. Define the terms noise margin, propagation delay and power dissipation of logic families. Compare TTL and CMOS logic families showing the values of above mentioned terms.
2. Draw the circuit and explain the operation of a TTL NAND gate
3. Compare TTL, CMOS logic families in terms of fan-in, fan-out and supply voltage

Course Outcome 4 (CO4) : Sequential Logic Circuits

1. Realize a T flip-flop using NAND gates and explain the operation with truth table,excitation table and characteristic equation
2. Explain a MOD 6 asynchronous counter using JK Flip Flop
3. Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control andexplain its working

Course Outcome 5 (CO5) : Logic Circuit Design using HDL

1. Design a 4-to-1 mux using gate level Verilog model.
2. Design a verilog model for a hald adder circuit. Make a one bit full adder by connectingtwo half adder models.
3. Compare concurrent signal assignment versus sequential signal assignment.

Syllabus

Module 1: Number Systems and Codes:

Binary and hexadecimal number systems; Methods of base conversions; Binary and hexadecimal arithmetic; Representation of signed numbers; Fixed and floating point numbers; Binary coded decimal codes; Gray codes; Excess 3 code. Alphanumeric codes: ASCII. Basics of verilog -- basic language elements: identifiers, data objects, scalar data types, operators.

Module 2: Boolean Postulates and Fundamental Gates

Boolean postulates and laws – Logic Functions and Gates De-Morgan‘s Theorems, Principle of Duality, Minimization of Boolean expressions, Sum of Products (SOP), Product of Sums (POS), Canonical forms, Karnaugh map Minimization. Modeling in verilog, Implementation of gates with simple verilog codes.

Module 3: Combinatorial and Arithmetic Circuits

Combinatorial Logic Systems - Comparators, Multiplexers, Demultiplexers, Encoder, Decoder. Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder. Modeling and simulation of combinatorial circuits with verilog codes at the gate level.

Module 4: Sequential Logic Circuits:

Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF, Conversion of Flipflops, Excitation table and characteristic equation. Implementation with verilog codes. Ripple and Synchronous counters and implementation in verilog, Shift registers-SIPO, SISO, PISO, PIPO. Shift Registers with parallel Load/Shift, Ring counter and Johnsons counter. Asynchronous and Synchronous counter design, Mod N counter. Modeling and simulation of flipflops and counters in verilog.

odule 5: Logic families and its characteristics:

TTL, ECL, CMOS - Electrical characteristics of logic gates – logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power-delay product. TTL inverter - circuit description and operation; CMOS inverter - circuit description and operation;

Structure and operations of TTL and CMOS gates; NAND in TTL and CMOS, NAND and NOR in CMOS.

Text Books:

1. Mano M.M, Ciletti M.D., ―Digital Design‖, Pearson India, 4th Edition. 2006
2. D.V. Hall, –Digital Circuits and Systems‖, Tata McGraw Hill, 1989
3. S. Brown, Z. Vranesic, –Fundamentals of Digital Logic with Verilog Design‖, McGraw Hill.
4. Samir Palnika r―Verilog HDL: A Guide to Digital Design and Syntheis‖, SunsoftPress.
5. R.P. Jain, –Modern digital Electronics‖, Tata McGraw Hill, 4th edition, 2009

Reference Books:

1. W.H. Gothmann, –Digital Electronics – An introduction to theory and practice‖, PHI, 2nd edition ,2006
2. Wakerly J.F., –Digital Design: Principles and Practices,‖ Pearson India, 4th 2008
3. A. Ananthakumar ,‖Fundamentals of Digital Circuits‖, Prentice Hall, 2nd edition,2016
4. Fletcher, William I., An Engineering Approach to Digital Design, 1st Edition, Prentice Hall India, 1980

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Number Systems and Codes**:	
1.1	Binary, octal and hexadecimal number systems; Methods of base conversions;	2
1.2	Binary, octal and hexadecimal arithmetic;	1
1.3	Representation of signed numbers; Fixed and floating point numbers;	3
1.4	Binary coded decimal codes; Gray codes; Excess 3 code :	1
1.5	Error detection and correction codes - parity check codes and Hamming code-Alphanumeric codes:ASCII	3
1.6	Verilog basic language elements: identifiers, data objects, scalar data types,operators	2
2	**Boolean Postulates and Fundamental Gates:**	
2.1	Boolean postulates and laws – Logic Functions and Gates, De-Morgan‘s Theorems, Principle of Duality	2
2.2	Minimization of Boolean expressions, Sum of Products (SOP), Product of Sums (POS)	2
2.3	Canonical forms, Karnaugh map Minimization	1
2.4	Gate level modelling in Verilog: Basic gates, XOR using NAND and NOR	2
3	**Combinatorial and Arithmetic Circuits**	
3.1	Combinatorial Logic Systems - Comparators, Multiplexers,	2

	Demultiplexers	
3.2	Encoder, Decoder, Half and Full Adders, Subtractors, Serial and ParallelAdders, BCD Adder	3
3.3	Gate level modelling combinational logic circuits in Verilog: half adder, full adder, mux, demux, decoder, encoder	3
4	**Sequential Logic Circuits:**	
4.1	Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF	2
4.2	Conversion of Flipflops, Excitation table and characteristic equation.	1
4.3	Ripple and Synchronous counters, Shift registers- SIPO.SISO,PISO,PIPO	2
4.4	Ring counter and Johnsons counter, Asynchronous and Synchronous counter design	3
4.5	Mod N counter, Random Sequence generator	1
4.6	Modelling sequential logic circuits in Verilog: flipflops, counters	2
5	**Logic families and its characteristics**:	
5.1	TTL,ECL,CMOS- Electrical characteristics of logic gates – logic levels andnoise margins, fan-out, propagation delay, transition time, power consumption and power-delay product.	3
5.2	TTL inverter - circuit description and operation	1
5.3	CMOS inverter - circuit description and operation	1
5.4	Structure and operations of TTL and CMOS gates; NAND in TTL, NAND and NOR in CMOS.	2

Simulation Assignments (ECT203)

The following simulations can be done in QUCS, KiCad or PSPICE.

BCD Adder

- Realize a one bit paraller adder, simulate and test it.
- Cascade four such adders to form a four bit parallel adder.
- Simulate it and make it into a subcircuit.
- Develop a one digit BCD adder, based on the subcircuit, simulate and test it

BCD Subtractor

- Use the above 4 -bit adder subcircuit, implement and simulate a one digit BCD subtractor.
- Test it with two BCD inputs

Logic Implementation with Multiplexer

- Develop an 8 : 1 multiplexer using gates, simulate, test and make it into a subcircuit.
- Use this subcircuit to implement the logic function $f(A, B, C) = \Sigma m(1, 3, 7)$

  Modify the truth table properly and implement the logic function

  $f(A, B, C, D) = \Sigma\, m(1, 4, 12, 14)$using one 8 : 1 multiplexer.

BCD to Seven Segment Decoder

- Develop a BCD to seven segment decoder using gates and make it into a sub circuit.
- Simulate this and test it.

Ripple Counters

- Understand the internal circuit of 7490 IC and develop it in the simulator.

  Make it into a subcircuit and simulate it. Observe the truth table and timing diagrams formod-5, mod-2 and mod-10 operation.
- Develop a mod-40 (mod-8 and mod-5) counter by cascading two such subcircuits.
- Simulate and observe the timing diagram and truth table.

Synchronous Counters

- Design and develop a 4-bit synchronous counter using J-K flip-flops.
- Perform digital simulation and observe the timing diagram and truth table.

Sequence Generator

- Connect D flip-flops to realize and 8-bit shift register and make it into a sub circuit.

  Sequence generator that relies on the polynomial $P(D) = D_7 + D_3 + 1$, with each D representdelay of one clock cycle
- Simulate and observe this maximal length pseudo random sequence.

Transfer Characteristics of TTL and CMOS Inverters

Develop a standard TTL circuit and perform sweep simulation and observe the transfer characteristics. Compute the threshold voltage and noise margins.

Develop and simulate standard CMOS inverter circuit and perform sweep simulation andobserve the transfer characteristics. Compute the threshold voltage and noise margins.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION,
Course Code:ECT203
Course : Logic Circuit Design

Time: 3 hours **Max. Marks:100**

PART A

Answer ***all*** questions. Each question carries ***3 marks***.

1. Convert 203.52_{10} to binary and hexadecimal .
2. Compare bitwise and logical verilog operators .
3. Prove that NAND and NOR are not associative.
4. Convert the expression ABCD+AB*C*+ACD to minterms.
5. Define expressions in Verilog with example.
6. Explain the working of a decoder.
7. What is race around condition?
8. Convert a T flip-flop to D flip-flop.
9. Define fan-in and fan-out of logic circuits.
10. Define noise margin and how can you calculate it?

PART B

Answer ***any one*** question from each module. Each question carries 14 marks.

MODULE I

11. a. Subtract 4610 from 10010 using 2's complement arithmetic. (8 marks) b. Give a brief description on keywords and identifiers in Verilog with example.(6 marks)

12. a. Explain the floating and fixed point representation of numbers. (8 marks)
    b. Explain the differences between programming lanuguages and HDLs (6 marks)

MODULE II

13. a. Simplify f (A, B, C, D) = ∑ m(4, 5, 7, 8, 9, 11, 12, 13, 15) using K-maps. (7 marks)
    b. Write a Verilog code for implementing above function (7 marks)

14. a. Write a Verilog code to implement the basic gates. (7 marks)
    b. Reduce the following Boolean function using K-Map and implement the simplified function using the logic gates
    f (A, B, C, D) = ∑(0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14) (7 marks)

Module III

15. a. Design a 3-bit magnitude comparator circuit. (8 marks)
    b. Write a Verilog description for a one bit full adder circuit. (6 marks)

16. a. Write a verilog code to implement 4:1 multiplexer (6 marks) b. Implement the logic function f (A, B, C) = ∑ m(0, 1, 4, 7) using 8 : 1 and 4 : 1 multiplexers. (8 marks)

Module IV

17. Design MOD 12 asynchronous counter using T flip-flop. (14 marks)

18. a. Explain the operation of Master Slave JK flipflop. (7 marks)
    b. Derive the ouput Qn+1 in Terms of Jn, Kn and Qn. (7 marks)

Module V

19. a. Explain in detail about TTL with open collector output configuration. (8 marks)
    b. Draw an ECL basic gate and explain. (6 marks)

20. a. Demonstrate the CMOS logic circuit configuration and characteristics in detail. (8 marks)
    b. Compare the characteristics features of TTL and ECL digital logic families. (6 marks)

ECT205	NETWORK THEORY	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to analyze the linear time invariant electronic circuits.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO1	Apply Mesh / Node analysis to obtain steady state response ofthe linear time invariant networks.
CO2	Apply Network Theorems to obtain steady state response of the linear time invariant networks.
CO3	Apply Laplace Transforms to determine the transient behavior of RLC networks.
CO4	Apply Network functions to analyze the single port and twoport networks.
CO5	Apply Network Parameters to analyze the single port and two port networks.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO1	3	3	2							2		2
CO2	3	3	2							2		2
CO3	3	3	2							2		2
CO4	3	3	2							2		2
CO5	3	3	2							2		2

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	10
Understand	20	20	20
Apply	20	20	70
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks

Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Obtain steady state response of the network using Mesh / node analysis.

1. Enumerate different types of sources in electronic networks.
2. Solve networks containing independent and dependent sources using Mesh / Node analysis.
3. Evolve the steady-state AC analysis of a given network using Mesh or Node analysis.

Course Outcome 2 (CO2) : Obtain steady state response of the network using Network Theorems.

1. Determine the branch current of the given network with dependent source using superposition theorem.
2. State and prove Maximum Power Transfer theorem.
3. Find the Thevenin‘s / Norton‘s equivalent circuit across the port of a given network having dependent source.

Course Outcome 3 (CO3): Determine the transient behaviour of network using Laplace Transforms

1. The switch is opened at t = 0 after steady state is achieved in given network. Find the expression for the transient output current.
2. Find the Laplace Transform of a given waveform.
3. In the given circuit, the switch is closed at t = 0 , connecting an energy source to the R,C,L circuit. At time t = 0, it is observed that capacitor voltage has an initial value. For the element values given, determine expression for output voltage after converting the circuit into transformed domain.

Course Outcome 4 (CO4): Apply Network functions to analyze the single port and twoport network.

1. What are the necessary conditions for a network driving point function and Transfer functions?

2. Evaluate the Driving point function and Transfer function for the given network,
3. Plot the poles and zeros of the given network.

Course Outcome 5 (C35): Apply Network Parameters to analyze the two port network.

1. Deduce the transmission parameters of two port network in terms of two port network parameters.
2. Define the condition for a two port network to be reciprocal.
3. Two identical sections of the given networks are connected in parallel. Obtain the two port network parameters of the combination.

SYLLABUS

Module 1 : Mesh and Node Analysis

Mesh and node analysis of network containing independent and dependent sources. Supermesh and Supernode analysis. Steady-state AC analysis using Mesh and Node analysis.

Module 2 : Network Theorems

Thevenin‘s theorem, Norton‘s theorem, Superposition theorem, Reciprocity theorem, Maximum power transfer theorem. (applied to both dc and ac circuits having dependent source).

Module 3 : Application of Laplace Transforms

Review of Laplace Transforms and Inverse Laplace Transforms, Initial value theorem &Final value theorem, Transformation of basic signals and circuits into s-domain.

Transient analysis of RL, RC, and RLC networks with impulse, step and sinusoidal inputs (with and without initial conditions). Analysis of networks with transformed impedance anddependent sources.

Module 4 : Network functions

Network functions for the single port and two port network. Properties of driving point and transfer functions. Significance of Poles and Zeros of network functions, Time domainresponse from pole zero plot. Impulse Function & Response. Network functions in thesinusoidal steady state, Magnitude and Phase response.

Module 5 : Two port network Parameters

Impedance, Admittance, Transmission and Hybrid parameters of two port network. Interrelationship among parameter sets. Series and parallel connections of two port networks.

Reciprocal and Symmetrical two port network. Characteristic impedance, Image impedance and propagation constant (derivation not required)

Text Books

1. Valkenburg V., ―Network Analysis‖, Pearson, 3/e, 2019.
2. Sudhakar A, Shyammohan S. P., ―Circuits and Networks- Analysis and Synthesis‖, McGraw Hill,5/e, 2015.

Reference Books

1. Edminister, ―Electric Circuits – Schaum‘s Outline Series‖, McGraw-Hill, 2009.
2. W. Hayt, J. Kemmerly, J. Phillips, S. Durbin, ―Engineering Circuit Analysis,‖ McGraw Hill.
3. K. S. Suresh Kumar, ―Electric Circuits and Networks‖, Pearson, 2008.
4. William D. Stanley, ―Network Analysis with Applications‖, 4/e, Pearson, 2006.
5. Ravish R., ―Network Analysis and Synthesis‖, 2/e, McGraw-Hill, 2015.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Mesh and Node Analysis**	
1.1	Review of circuit elements and Kirchhoff‘s Laws	2
1.2	Independent and dependent Sources, Source transformations	1
1.3	Mesh and node analysis of network containing independent and dependent sources	3
1.4	Supermesh and Supernode analysis	1
1.5	Steady-state AC analysis using Mesh and Node analysis	3
2	**Network Theorems (applied to both dc and ac circuits having dependent source)**	
2.1	Thevenin‘s theorem	1
2.2	Norton‘s theorem	1
2.3	Superposition theorem	2
2.4	Reciprocity theorem	1
2.5	Maximum power transfer theorem	2
3	**Application of Laplace Transforms**	
3.1	Review of Laplace Transforms	2
3.2	Initial value theorem & Final value theorem (Proof not necessary)	1
3.3	Transformation of basic signals and circuits into s-domain	2
3.4	Transient analysis of RL, RC, and RLC networks with impulse, step, pulse, exponential and sinusoidal inputs	3
3.5	Analysis of networks with transformed impedance and dependent sources	3
4	**Network functions**	
4.1	Network functions for the single port and two port network	2
4.2	Properties of driving point and transfer functions	1

4.3	Significance of Poles and Zeros of network functions, Time domain response from pole zero plot	1
4.4	Impulse Function & Response	1
4.5	Network functions in the sinusoidal steady state, Magnitude and Phase response	3
5	**Two port network Parameters**	
5.1	Impedance, Admittance, Transmission and Hybrid parameters of two port network	4
5.2	Interrelationship among parameter sets	1
5.3	Series and parallel connections of two port networks	2
5.4	Reciprocal and Symmetrical two port network	1
5.5	Characteristic impedance, Image impedance and propagation constant (derivation not required)	1

Simulation Assignments:

At least one assignment should be simulation of steady state and transient analysis of R, L, C circuits with different types of energy sources on any circuit simulation software. Samples of simulation assignments are listed below. The following simulations can be done in QUCS, KiCad or PSPICE.

1. Make an analytical solution of Problem 4.3 in page 113 of the book *Network Analysis* by M EVan Valkenberg. Realize this circuit in the simulator and observe *i(t)* and V_2 *(t*) using transient simulation.

2. Realize a series RLC circuit with

- R = 200Ω, L = 0.1H, C = 13.33μF
- R = 200Ω, L = 0.1H, C = 10μF and
- R = 200Ω, L = 0.1H, C = 1μF and no source respectively. The initial voltage across the capacitor is 200V Simulate the three circuits, and observe the current *i(t)* through them.

3. Repeat the above assignment for the three set of component values for a parallel RLC circuit.

4. Refer Problem 9.18 in page 208 in the book *Electric Circuits* by Nahvi and Edminister 4th Edition. See Fig. 9.28. Simulate this circuit to verify superposition theorem for the three current with individual sources and combination.

5. Refer Problem 9.22 in page 210 in the book *Electric Circuits* by Nahvi and Edminister 4th Edition. See Fig. 9.32. Implement the circuit on the simulator with V = 30< 30°. Verify the duality between the sources V and the current *I2* and *I3* using simulation.

6. See Fig. 12.40 in Chapter 12 (page 298) in the above book. Let R1 = R2 = 2kΩ, L = 10mH and C = 40nF. Implement this circuit in the simulator and perform the ac analysisto plot the frequency response.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION,

Course Code:ECT205

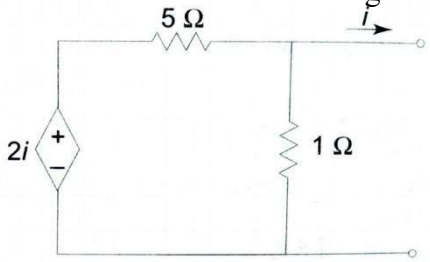
Course: NETWORK THEORY

Time: 3 hours **Max. Marks:100**

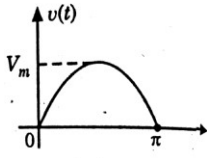
PART A

Answer ***all*** questions. Each question carries ***3 marks***.

1. Illustrate the source-transformation techniques.
2. Explain the concept of super node.
3. State and prove Maximum Power Transfer theorem
4. Evaluate the Norton's equivalent current in the following circuit.



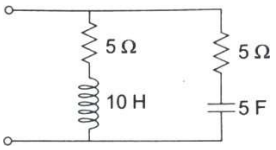
5. Evaluate the Laplace Transform of half-wave rectified sine pulse



6. Give the two forms of transformed impedance equivalent circuit of a capacitor with initial charge across it.

7 Enumerate necessary condition for a Network Functions to be Transfer Functions.

8 Obtain the pole zero configuration of the impedance function of the followingcircuit.



9 Define the short-circuit admittance parameter with its equivalent circuit.

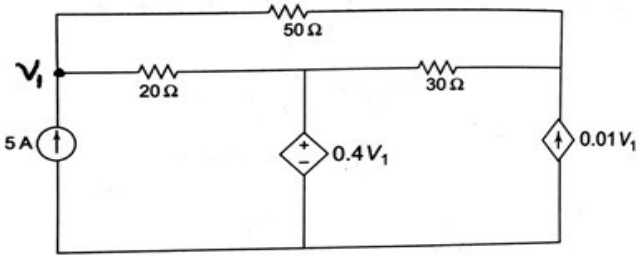
10 Deduce Z-parameter in terms of h-parameter.

PART B

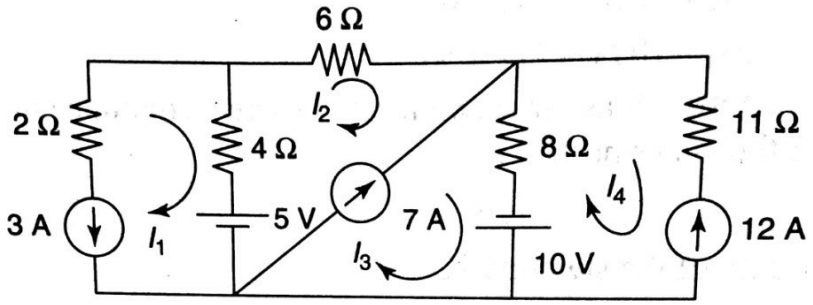
Answer ***any one*** question from each module. Each question carries 14 marks.

MODULE I

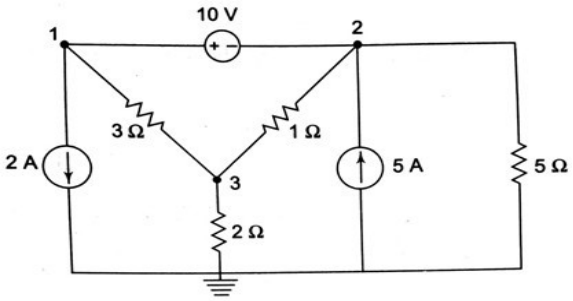
11 a. Find the voltage V_1 using nodal analysis. (7 marks)



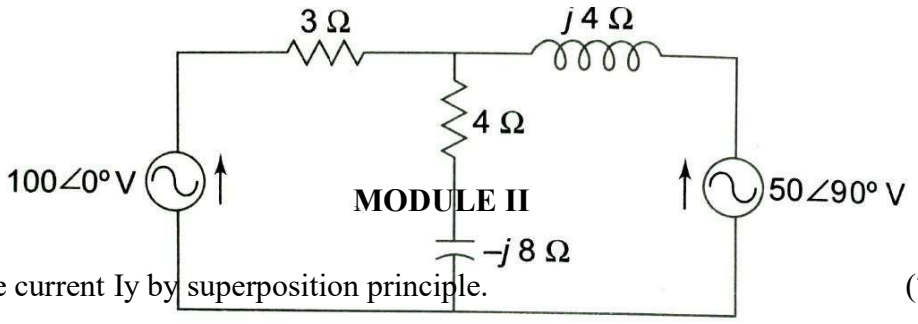
b. Find the current through 8 ohms resistor in the following circuit using mesh analysis. (7 marks)



12 a. Find the power delivered by the 5A current source using nodal analysis method. (7 marks)

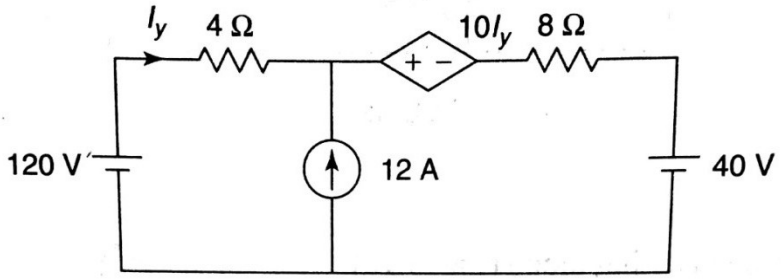


b. Determine the values of source currents using Mesh analysis (7marks)

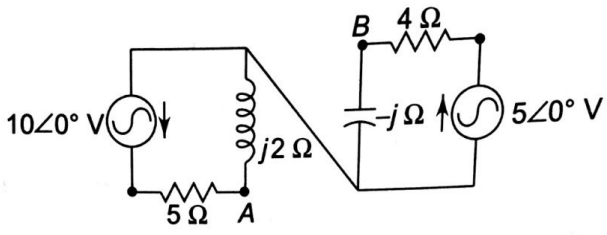


MODULE II

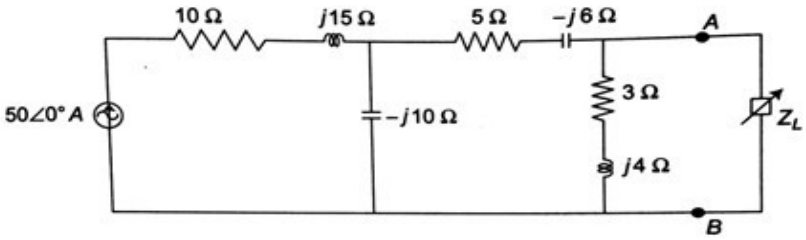
13 a. Find the current Iy by superposition principle. (7marks)



b. Find the Norton's equivalent circuit across the port AB. (7marks)

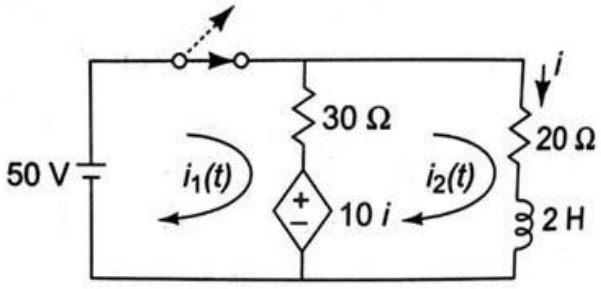


14 Determine the maximum power delivered to the load in the circuit. (14 marks)



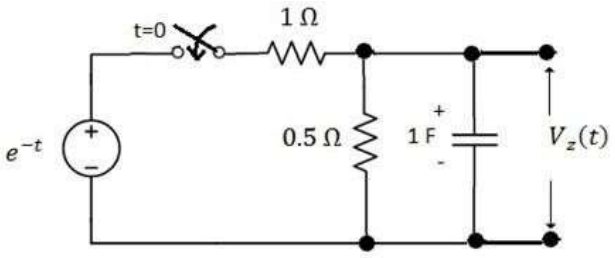
MODULE III

15 a. The switch is opened at t = 0 after steady state is achieved. Find the expression for the transient current i. (8 marks)



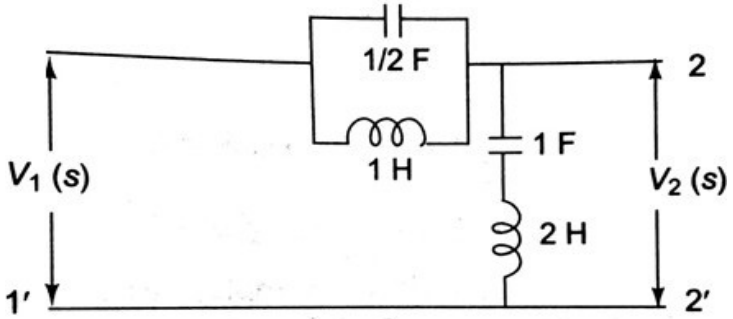
b. A voltage pulse of unit height and width _ T ‘ is applied to a low pass RC circuit at time t=0.Determine the expression for the voltage across the capacitor C as a function of time. (6 marks)

16 In the circuit, the switch is closed at t = 0 , connecting a source e^{-t} to the RC circuit. At time ,t = 0 it is observed that capacitor voltage has the value $V_c = 0.5V$. For the element values given, determine V_z (t) after converting the circuit into transformed domain. (14 marks)



MODULE IV

17 For the network, determine Driving point impedance $Z_{11}(s)$, Voltage gain Transfer function G_{21} (s) and Current gain Transfer function α_{21} (s). (14 marks)



18 Compare and contrast the necessary conditions for a network driving point function and Transfer functions. (7 marks)

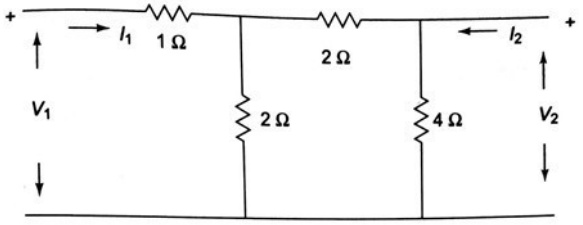
b. For following network, evaluate the admittance function Y(s) as seen by the source i(t). Also pot the poles and zeros of Y(s). (7 marks)

MODULE V

19. a. Deduce the transmission parameters of two port network in terms of (i) Z-parameters, (ii) Y-parameters and (iii) Hybrid parameters. (10 marks)

b. How to determine the given two port network is Symmetrical (4 marks)

20 Two identical sections of the following networks are connected in parallel. Obtain the Y parameters of the combination. (14 marks)



ECL201	SCIENTIFIC COMPUTING LABORATORY	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble:

- The following experiments are designed to translate the mathematical concepts into system design
- The students shall use Python for realizing experiments. Other softwares such as R/MATLAB/SCILAB/LabVIEW can also be used.
- The experiments will lay foundation for future labs such as DSP.
- The first two experiments are mandatory and any six of the rest should be done.

Prerequisite:

- MAT 101 Linear Algebra and Calculus
- MAT 102 Vector Calculus, Differential Equations and Transforms

Course Outcomes: After the completion of the course the student will be able to

CO1	Describe the needs and requirements of scientific computing and to familiarize one programming language for scientific computing anddata visualization.
CO2	Approximate an array/matrix with matrix decomposition.
CO3	Implement numerical integration and differentiation.
CO4	Solve ordinary differential equations for engineering applications
CO5	Compute with exported data from instruments
CO6	Realize how periodic functions are constituted by sinusoids
CO7	Simulate random processes and understand their statistics.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO1	3	3	3	2	3	0	0	0	3	1	0	3
CO2	3	3	1	2	3	0	0	0	3	0	0	1
CO3	3	3	1	1	3	0	0	0	0	0	0	1
CO4	3	3	1	1	3	0	0	0	0	0	0	1
CO5	3	3	1	3	0	0	0	0	3	3	0	0
CO6	3	3	2	2	3	0	0	0	3	1	0	0
CO7	3	3	2	2	3	0	0	0	3	1	0	1

Assessment Pattern

Mark distribution

Total Marks	CIE	ESE
150	75	75

Continuous Internal Evaluation Pattern:

Attribute	Mark
Attendance	15
Continuous assessment	30
Internal Test (Immediately before the second series test)	30

End Semester Examination Pattern: The following guidelines should be followed regarding award of marks.

Attribute	Mark
Preliminary work	15
Implementing the work/Conducting the experiment	10
Performance, result and inference (usage of equipments and trouble shooting)	25
Viva voce	20
Record	5

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Level Assessment Questions

CO1-The needs and requirements of scientific computing and to familiarize one programming language for scientific computing and data visualization

1. Write a function to compute the first *N* Fibonacci numbers. Run this code and test it.
2. Write a function to compute the sum of *N* complex numbers. Run this code and test it.
3. Write a function to compute th factorial of an integer. Run this code and test it.

CO2-Approximation an array/matrix with matrix decomposition.

1. Write a function to compute the eigen values of a real valuedmatrix (say 5 5). Run this code. Plot the eigen values and understand their variation.
2. Write a function to approximate a 5 5 matrix using its first 3 eigen vales. Run the code and compute the absolute square error in the approximation.

CO3-Numerical Integration and Differentiation

1. Write and execute a function to return the first and second derivative of the function $f(t) = 3t^4 + 5$ for the vector $t = [-3, 3]$.

2. Write and execute a function to return the value of $\int_{-3}^{3} e^{-|t|}\, dt$

CO4-Solution of ODE

1. Write and execute a function to return the numerical solution of

$$\frac{d^2x}{dt^2} + 4\frac{dx}{dt} + 2x = e^{-t}\cos(t)$$

2. Write and execute a function to solve for the current transient through an RL network (with r/L = 1) that is driven by the signal $5e^{-t}U(t)$

CO5-Data Analysis

1. Connect a signal generator to a DSO and display a $1\ V$, $3\ kHz$ signal. Store the trace in a usb device as a spreadsheet. Write and execute a function to load and display signal from the spreadsheet. Compute the rms value of the signal.

2. Write and execute a program to display random data in two dimensions as continuous and discrete plots.

CO6-Convergence of Fourier Series

1. Write the Fourier series of a traingular signal. Compute this sum for 10 and 50 terms respectively. Plot both signals on the same GUI.

CO7-Simulation of Random Phenomena

1. Write and execute a function to toss three fair coins simultaneously.Compute the probability of getting exactly two heads for 100 and 1000 number of tosses

Experiments

Experiment 1. Familiarization of the Computing Tool

1. Needs and requirements in scientific computing

2. Familiarization of a programming language like Python/R/ MATLAB/ SCILAB/ LabVIEW for scientific computing

3. Familiarization of data types in the language used.

4. Familiarization of the syntax of while, for, if statements.

5. Basic syntax and execution of small scripts.

Experiment 2. Familiarization of Scientific Computing

1. Functions with examples
2. Basic arithmetic functions such as abs, sine, real, imag, complex, sinc etc. using bulit in modules.
3. Vectorized computing without loops for fast scientific applications.

Experiment 3. Realization of Arrays and Matrices

1. Realize one dimensional array of real and complex numbers
2. Stem and continous plots of real arrays using matplotlib/GUIs/charts.
3. Realization of two dimensional arrays and matrices and their visualizations with imshow/ matshow/ charts
4. Inverse of a square matrix and the solution of the matrix equation[**A**][**X**] = [**b**] where **A** is an $N \times N$ matrix and **X** and **b** are $N \times 1$ vectors.
5. Computation of the rank (ρ) and eigen values (λ_i) of **A**
6. Approximate A for N = 1000 with the help of singular value composition of A as $\tilde{A} = \sum_{i=0}^{r} \lambda_i U_i V^T$ where U_i and V_i are the singular vectors and λ_i are the eigen values with $\lambda_i < \lambda_j$ for $i > j$. One may use the built-in functions for singular value decomposition.
7. Plot the absolute error(ζ) between $\mathbf{A}$ and $\tilde{\mathbf{A}}$ as

$$\zeta = \sum_{i=1}^{N} \sum_{j=1}^{N} |a_{i,j} - \tilde{a}_{i,j}|^2$$

against r for r = 10, 50, 75, 100, 250 , 500, 750 and appreciate the plot.

Experiment 4. Numerical Differentiation and Integration

1. Realize the functions sin t, cos t, sinht and cosht for the vector t =[0; 10] with increment 0.01
2. Compute the first and second derivatives of these functions using built in tools such as grad.
3. Plot the derivatives over the respective functions and appreciate.
4. Familiarize the numerical integration tools in the language you use.
5. Realize the function $f(t) = 4t^2 + 3$ and plot it for the vector t = [-5; 5] with increment 0.01

6. Use general integration tool to compute $\int_{-2}^{2} f(t)dt$

7. Repeat the above steps with trapezoidal and Simpson method and compare the results.

8. Compute $\frac{1}{\sqrt{2\pi}}\int_{0}^{\alpha} e^{\frac{-x^2}{2}} dx$ using the above three methods.

Experiment 5. Solution of Ordinary Differential Equations

1. Solve the first order differential equation $\frac{dx}{dt} + 2x = 0$ with initial condition x(0) = 1

2. Solve for the current transient through an RC network (with RC = 3) that is driven by

    - 5 V DC
    - the signal $5e^{-t}U(t)$ and plot the solutions.

3. Solve the second order differential equation $\frac{d^2x}{dt^2} + 2\frac{dx}{dt} + 2x = e^{-t}$

4. Solve the current transient through a series RLC circuit with R = 1 Ω,L = 1mH and C = 1 μ F that is driven by

    - 5 V DC
    - the signal $5e^{-t}U(t)$.

Experiment 6. Simple Data Visualization

1. Draw stem plots, line plots, box plots, bar plots and scatter plots with random data.

2. plot the histogram of a random data.

3. create legends in plots.

4. Realize a vector t = [-10; 10] with increment 0.01 as an array.

5. Implement and plot the functions

    - f(t) = cos t
    - f(t) = cos t cos 5t + cos 5t

Experiment 7. Simple Data Analysis with Spreadsheets

1. Display an electrical signal on DSO and export it as a .csv file.

2. Read this .csv or .xls file as an array and plot it.

3. Compute the mean and standard deviation of the signal. Plot its histogram with an appropriate bin size.

Experiment 8. Convergence of Fourier Series

The experiment aims to understand the lack of convergence of Fourier series

1. Realize the Fourier series

$$f(t) = 4/\pi\,[1 - 1/3\cos 2\pi 3t/T + 1/5\cos 2\pi 5t/T - 1/7\cos 2\pi 7t/T + \cdots]$$

2. Realize the vector t = [0; 100] with an increment of 0.01 and keep T = 20.
3. Plot the first 3 or 4 terms on the same graphic window and understand how the smooth sinusoids add up to a discontinuous square function.
4. Compute and plot the series for the first 10, 20, 50 and 100 terms of the and understand the lack of convergence at the points of discontinuity.
5. With t made a zero vector, f(0) = 1, resulting in the Madhava series for π as

$$\pi = 4[1 - 1/3 + 1/5 - 1/7 + \cdots]$$

6. Use this to compute π for the first 10, 20, 50 and 100 terms.

Experiment 9: Coin Toss and the Level Crossing Problem

1. Simulate a coin toss that maps a head as 1 and tail as 0.
2. Toss the coin N = 100, 500,1000, 5000 and 500000 times and compute the probability (p) of head in each case.
3. Compute the absolute error |0.5 – p| in each case and plot against N and understand the law of large numbers.
4. Create a uniform random vector with maximum magnitude 10, plot and observe.
5. Set a threshold (VT = 2) and count how many times the random function has crossed VT.
6. Count how many times the function has gone above and below the threshold.

Schedule of Experiments: Every experiment should be completed in three hours.

ECL203	LOGIC DESIGN LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble:

This course aims to

(i) familiarize students with the Digital Logic Design through the implementation of Logic Circuits using ICs of basic logic gates

(ii) Familiarize studentswith the HDL based Digital Design Flow.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO1	Design and demonstrate the functioning of various combinational and sequential circuits using ICs
CO2	Apply an industry compatible hardware description language to implement digital circuits
CO3	Implement digital circuis on FPGA boards and connect external hardware to the boards
CO4	Function effectively as an individual and in a team to accomplish the given task

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO1	3	3	3						3			3
CO2	3	1	1	3	3				3			3
CO3	3	1	1	3	3				3	1		3
CO4	3	3	3		3				3			3

Assessment Pattern

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	75	75	2.5Hrs

Continuous Internal Evaluation Pattern:

Attribute	Mark
Attendance	15
Continuous assessment	30
Internal Test (Immediately before the second series test)	30

End Semester Examination Pattern: The following guidelines should be followed regarding award of marks.

Attribute	Mark
Preliminary work	15
Implementing the work/Conducting the experiment	10
Performance, result and inference (usage of equipments and trouble shooting)	25
Viva voce	20
Record	5

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Level Assessment Questions

Course Outcome 1 (CO1): Design and Development of combinational circuits

1. Design a one bit full adder using gates and implement and test it on board.
2. Implement and test the logic function $f(A,B,C)=\sum m(0,1,3,6)$ using an 8:1 Mux IC
3. Convert a D flip-flop to T flip-flop and implement and test on board.

Course Outcome 2 and 3 (CO2 and CO3): Implementation of logic circuits on tiny FPGA

1. Design and implement a one bit subtracter in Verilog and implement and test it on a tiny FPGA board.
2. Design and implement a J-K flip-flop in Verilog, implement and test it on a tiny FPGA board.
3. Design a 4:1 Multiplexer in Verilog and implement and test it on tiny FPGA board.

List of Experiments:

It is compulsory to conduct a minimum of 5 experiments from Part A and a minimum of 5 experiments from Part B.

Part A (Any 5)

The following experiments can be conducted on breadboard or trainer kits.

1. Realization of functions using basic and universal gates (SOP and POS forms).

2. Design and Realization of half /full adder and subtractor using basic gates and universal gates.
3. 4 bit adder/subtractor and BCD adder using 7483.
4. Study of Flip Flops: S-R, D, T, JK and Master Slave JK FF using NAND gates.
5. Asynchronous Counter:3 bit up/down counter
6. Asynchronous Counter:Realization of Mod N counter
7. Synchronous Counter: Realization of 4-bit up/down counter.
8. Synchronous Counter: Realization of Mod-N counters.
9. Ring counter and Johnson Counter. (using FF & 7495).
10. Realization of counters using IC‘s (7490, 7492, 7493).
11. Multiplexers and De-multiplexers using gates and ICs. (74150, 74154)
12. Realization of combinational circuits using MUX & DEMUX.
13. Random Sequence generator using LFSR.

PART B (Any 5)

The following experiments aim at training the students in digital circuit design with verilog and Implementation in small FPGAs. Small, low cost FPGAs, that can be driven by open tools for simulation, synthesis and place and route, such as Tiny FPGA or Lattice iCEstick can be used. Open software tools such as yosis (for simulation and synthesis) and arachne (for place and route) may be used. The experiments will lay the foundation for digital design with FPGA with the objective of increased employability.

Experiment 1. Realization of Logic Gates and Familiarization of FPGAs

(a) Familiarization of a small FPGA bboard and its ports and interface.

(b) Create the .pcf files for your FPGA board.

(c) Familiarization of the basic syntax of verilog

(d) Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables.

(e) Verify the universality and non associativity of NAND and NOR gates by uploading the corresponding verilog files to the FPGA boards.

Experiment 2: Adders in Verilog

(a) Development of verilog modules for half adder in 3 modeling styles (dataflow/structural/ behavioral).

(b) Development of verilog modules for full adder in structural modeling using half adder.

Experiment 3: Mux and Demux in Verilog

(a) Development of verilog modules for a 4x1 MUX.

(b) Development of verilog modules for a 1x4 DEMUX.

Experiment 4: Flipflops and counters

(a) Development of verilog modules for SR, JK and D flipflops.

(b) Development of verilog modules for a binary decade/Johnson/Ring counters

Experiment 5. Multiplexer and Logic Implementation in FPGA

(a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality.

(b) Use the above module to realize the logic function f (A, B, C) = ∑m(0, 1, 3, 7) and test it.

(c) Use the same 8 : 1 multiplexer to realize the logic function f (A, B, C, D) = ∑m(0, 1, 3, 7, 10, 12) by partitioning the truth table properly and test it.

Experiment 6: Flip-Flops and their Conversion in FPGA

(a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board.

(b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D

Experiment 7: Asynchronous and Synchronous Counters in FPGA

(a) Make a design of a 4-bit up down ripple counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board.

(b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board.

Experiment 8: Universal Shift Register in FPGA

(a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board.

(b) Implement ring and Johnson counters with it.

Experiment 9. BCD to Seven Segment Decoder in FPGA

(a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality.

(b) Test it with switches and seven segment display. Use ouput ports for connection to the display

SEMESTER - 4

ECT202	**ANALOG CIRCUITS**	**CATEGORY**	**L**	**T**	**P**	**CREDIT**
		PCC	3	1	0	4

Preamble: This course aims to develop the skill of analyze and design of different types of analog circuits using discrete electronic components.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO1	Design analog signal processing circuits using diodes and first order RC circuit.
CO2	Analyze basic amplifiers using BJT.
CO3	Analyze basic amplifiers using MOSFET.
CO4	Analyze basic feedback amplifiers and oscillators using BJT and MOSFET
CO5	Design power amplifiers and regulated power supply circuits.

Mapping of course outcomes with program outcomes

	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO12**
CO1	3	3	2		1							3
CO2	3	3	2		1							3
CO3	3	3	2		1							3
CO4	3	3	2		1							3
CO5	3	3	2		1							3

Assessment Pattern

Bloom's Category	**Continuous Assessment Tests**		**End Semester Examination**
	1	**2**	
Remember	10	10	10
Understand	20	20	20
Apply	20	20	70
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks

Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Design analog signal processing circuits using diodes and first order RC circuit.

1. For the given specification design a differentiator / integrator circuit.
2. For the given transfer characteristics design clipping / clamping circuit.
3. Design first order RC low-pass / high-pass circuit for the given specification.

Course Outcome 2 (CO2): Analyze basic amplifiers using BJT.

1. For the given transistor biasing circuit, determine the resistor values, biasing currents and voltages.
2. Design a RC coupled amplifier for a given gain.
3. Analyze the frequency response of BJT RC coupled amplifier using hybrid π model.

Course Outcome 3 (CO3): Analyze basic amplifiers using MOSFET.

1. Perform DC analysis of MOSFET circuits.
2. Design a common source amplifier.
3. Deduce the expression for voltage gain of CS stage with diode-connected load.

Course Outcome 4 (CO2): Analyze basic feedback amplifiers and oscillators.

1. Deduce the expression for voltage gain, input impedance and output impedance of the four feedback amplifier topologies.
2. Design practical discrete amplifiers for the four feedback amplifier topologies.
3. Design oscillator using BJT to generate sine wave for the given frequency.

Course Outcome 3 (CO3): Apply the principle of power amplifiers and regulated power supply.

1. Design power amplifiers of different classes using BJT.
2. Deduce the expression for maximum efficiency of class B power amplifiers.
3. Illustrate the DC and AC load line in transformer coupled class A power amplifiers.
4. Design voltage regulator for the given specifications.

SYLLABUS

Module 1:

Wave shaping circuits: First order RC differentiating and integrating circuits, First order RC

low pass and high pass filters. Diode Clipping circuits - Positive, negative and biased clipper. Diode Clamping circuits - Positive, negative and biased clamper.

Transistor biasing: Need, operating point, concept of DC load line, fixed bias, self bias, voltage divider bias, bias stabilization.

Module 2:

BJT Amplifiers: RC coupled amplifier (CE configuration) – need of various components and design, Concept of AC load lines, voltage gain and frequency response. Small signal analysis of CE configuration using small signal hybrid-pi model for mid frequency and low frequency. (gain, input and output impedance).

High frequency equivalent circuits of BJT, Miller effect, Analysis of high frequency response of CE amplifier.

Module 3:

MOSFET amplifiers: MOSFET circuits at DC, MOSFET as an amplifier, Biasing of discrete MOSFET amplifier, small signal equivalent circuit. Small signal voltage and current gain, input and output impedance of CS configuration. CS stage with current source load, CS stage with diode-connected load.

Multistage amplifiers - effect of cascading on gain and bandwidth. Cascode amplifier.

Module 4 :

Feedback amplifiers: Effect of positive and negative feedback on gain, frequency response and distortion. The four basic feedback topologies, Analysis of discrete BJT circuits in voltage-series and voltage-shunt feedback topologies - voltage gain, input and output impedance.

Oscillators: Classification, criterion for oscillation, Wien bridge oscillator, Hartley and Crystal oscillator. (working principle and design equations of the circuits; analysis of Wien bridgeoscillator only required).

Module 5:

Power amplifiers: Classification, Transformer coupled class A power amplifier, push pull class B and class AB power amplifiers, complementary-symmetry class B and Class AB power amplifiers, efficiency and distortion (no analysis required)

Regulated power supplies: Shunt voltage regulator, series voltage regulator, Short circuit protection and fold back protection, Output current boosting.

Text Books

1. Robert Boylestad and L Nashelsky, ―Electronic Devices and Circuit Theory‖, 11/e Pearson, 2015.

2. Sedra A. S. and K. C. Smith, ―Microelectronic Circuits‖, 6/e, Oxford University Press, 2013.

Reference Books

1. Razavi B., ―Fundamentals of Microelectronics‖, Wiley, 2015

2. Neamen D., ―Electronic Circuits, Analysis and Design‖, 3/e, TMH, 2007.

3. David A Bell, ―Electronic Devices and Circuits‖, Oxford University Press, 2008.

4. Rashid M. H., ―Microelectronic Circuits - Analysis and Design‖, Cengage Learning,2/e,2011

5. Millman J. and C. Halkias, ―Integrated Electronics‖, 2/e, McGraw-Hill, 2010

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Wave shaping circuits**	**(9)**
1.1	Analysis and design of RC differentiating and integrating circuits	2
1.2	Analysis and design of First order RC low pass and high pass filters	2
1.3	Clipping circuits - Positive, negative and biased clipper	1
1.4	Clamping circuits - Positive, negative and biased clamper	1
	Transistor biasing	
1.5	Need of biasing, operating point, bias stabilization, concept of load line	1
1.6	Design of fixed bias, self bias, voltage divider bias. Mesh and Node Analysis	2
2	**BJT Amplifiers**	**(9)**
2.1	Classification of amplifiers, RC coupled amplifier (CE configuration) – need of various components and design, Concept of AC load lines.	2
2.2	Small signal analysis of CE configuration using small signal hybrid π model for mid frequency. (gain, input and output impedance).	3
2.3	High frequency equivalent circuits of BJT, Miller effect, Analysis of high frequency response of CE amplifier. voltage gain and frequency response	4
3	**MOSFET amplifiers**	**(10)**
3.1	MOSFET circuits at DC, MOSFET as an amplifier, Biasing of discrete MOSFET amplifier	2
3.2	Small signal equivalent circuit. Small signal voltage and current gain, input and output impedances of CS configuration	3
3.3	CS stage with current source load, CS stage with diode-connected load.	2
3.4	**Multistage amplifiers** - effect of cascading on gain and bandwidth. Cascode amplifier.	3
4	**Feedback amplifiers**	**(9)**
4.1	Properties of positive and negative feedback on gain, frequency response and	1

	distortion.	
4.2	Analysis of the four basic feedback topologies	2
4.3	Analysis of discrete circuits in each feedback topologies –voltage gain, input and output impedance	3
	Oscillators	
4.4	Classification, criterion for oscillation	1
4.5	Wien bridge oscillator, Hartley and Crystal oscillator. (working principle and design equations of the circuits; analysis not required).	2
5	**Power amplifiers**	
5.1	Classification, Transformer coupled class A power amplifier	1
5.2	push pull class B and class AB power amplifiers, complementary symmetry class B and Class AB power amplifiers, efficiency and distortion (no analysis required)	3
	Linear Regulated power supplies	
5.3	Principle of Linear Regulated power supplies, Shunt voltage regulator	1
5.4	Series voltage regulator, Short circuit protection and fold back protection, Output current boosting	2

Simulation Assignments:

At least one assignment should be simulation of different types of transistor amplifiers on any circuit simulation software.

The following simulations can be done in QUCS, KiCad or PSPICE.

1. Design and simulate a voltage series feedback amplifier based on BJT/ MOSFET. Observe the input and output signals. Plot the AC frequency response. Observe the Nyquist plot and understand its stability.
2. Design and simulate a voltage shunt feedback amplifier based on BJT/ MOSFET. Observe the input and output signals. Plot the AC frequency response. Observe the Nyquist plot and understand its stability
3. Design and simulate series voltage regulator for output voltage VO = 10V and output current IO = 100mA with and without short circuit protection and to test the line and load regulations.
4. Design and simulate Wien bridge oscillator for a frequency of 5 kHz. Run a transient simulation and observe the output waveform.
5. Design and simulate Colpitts oscillator for a frequency of 455 kHz. Run a transient simulation and observe the output waveform.
6. Design and simulate a current series feedback amplifier based on BJT. Observe the input and output signals. Plot the AC frequency response. Observe the Nyquist plot and understand its stability
7. Design and simulate Hartley oscillator for a frequency of 455 kHz. Run a transient simulation and observe the output waveform.
8. Design and simulate clipping circuits that clips the 10 V input sinusoid
   at +3.5 V and at -4.2 V
   at +2.5 V and at +4.2 V
   at – 2.5 V and at - 4: V

with Si diodes

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION,

Course Code: ECT202

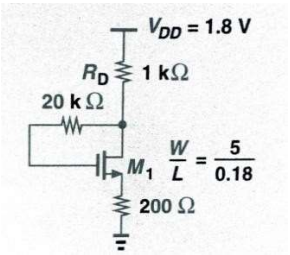
Course: Analog Circuits

Time: 3 hours **Max. Marks:100**

PART A

Answer ***all*** questions. Each question carries ***3 marks***.

1. Design the first order RC high pass filter with cut off frequency 2Kz.
2. Describe about the double ended clipping.
3. Differentiate between DC and AC load lines.
4. What is the significance of Miller effect on high frequency amplifiers?
5. What are the effects of cascading in gain and bandwidth of an amplifier?
6. Calculate the drain current if μnCox = 100 μA/V2, VTH = 0.5V and λ = 0 in the following circuit.



7. Illustrate the effect of negative feedback on bandwidth and gain of the amplifier.
8. Explain the criteria for an oscillator to oscillate.
9. How to eliminate cross over distortion in class-B power amplifier?
10. What is line regulation and load regulation in the context of a voltage regulator?

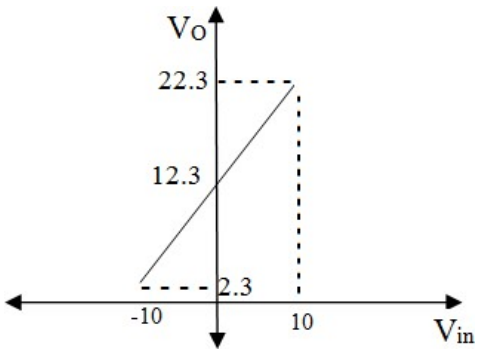
PART – B

Answer one question from each module; each question carries 14 marks.

Module - I

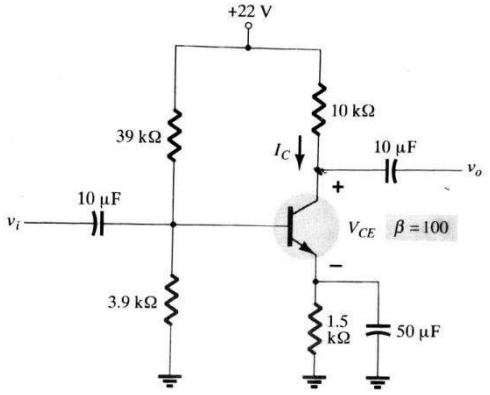
11 a. Design a differentiator circuit for a square wave signal with Vpp=10 and frequency 10KHz. (6 marks)

b. Design a clamper circuit to get the following transfer characteristics, assuming voltage drop across the diodes 0.7V. (8 marks)



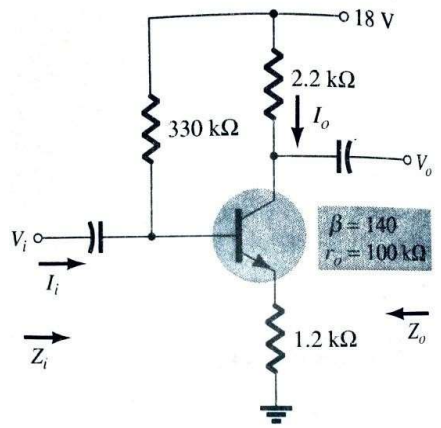
12 a. Explain the working of an RC differentiator circuit for a square wave input with period T. Sketch its output waveform for RC T, ≫ T, RC ≪ T and RC = T. (5 marks)

b. With reference to the following circuit, draw the load line and mark the Q point of the Silicon BJT transistor. (9 marks)



Module – II

13. For the following RC coupled amplifier determine re , Zi , Zo and Av . (14 marks)



14. a. Draw the high frequency hybrid π model of BJT in CE configuration and explain the significance of each parameter. (6 marks)

b. Analyze BJT RC coupled amplifier in CE configuration at high frequency using hybrid π model. (8 marks)

Module – III

15 a. Draw the circuit of a common source amplifier using MOSFET. Derive the expressions for voltage gain and input resistance from small signal equivalent circuit. (7 marks)

b. How wide bandwidth is obtained in Cascode amplifier ? (7 marks)

16 a. Draw the CS stage with current source load and deduce the expression for voltage gain of the amplifier. (14marks)

Module – IV

17 Give the block schematic of current-series feedback amplifier configuration and deduce the expression for gain, input impedance and output impedance with feedback. Design a practical circuit for this current-series feedback amplifier. (14 marks)

18 a. Design wein-bridge oscillator using BJT to generate 1KHz sine wave. (8 marks)
b Explain the working principle of crystal oscillator (7 marks)

Module – V

19 Illustrate the working principle of complementary-symmetry class B power amplifiers and deduce the maximum efficiency of the circuit (14 marks)

20 Design a discrete series voltage regulator with short circuit protection for regulated output voltage 10V and maximum current 100mA. (14 marks)

EVT204	DIGITAL SYSTEM DESIGN	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to design hazard free synchronous and asynchronous sequential circuits and implement the same in the appropriate hardware device.

Prerequisite: Logic Circuit Design

Course Outcomes: After the completion of the course the student will be able to

CO1	Analyze clocked synchronous sequential circuits
CO2	Analyze asynchronous sequential circuits
CO3	Design hazard free circuits
CO4	Diagnose faults in digital circuit
CO5	Analyze the role of HDLs in modeling and simulation of digital circuits in the VLSI design flow

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO1	3	3	3		2				2	2		3
CO2	3	3			2				2	2		3
CO3	3	3	3	3					2	2		3
CO4	3	2		1					2	2		3
CO5	3	3	3		2				2	2		2

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	15
Understand	10	20	30
Apply	20	20	35
Analyse	10		20
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks

Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

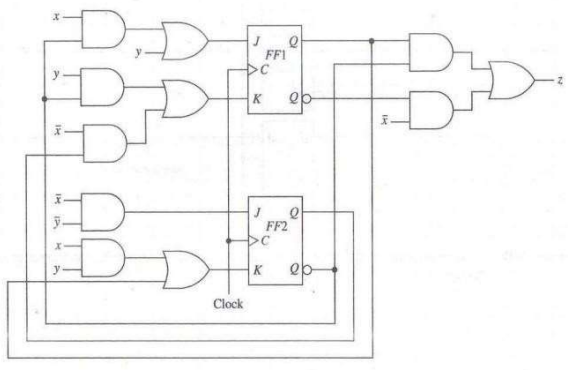
Course Level Assessment Questions

Course Outcome 1 (CO1): Analyze clocked synchronous sequential circuits

1. Construct an ASM chart for a sequence recognizer to recognize the input sequence of pairs x1x2= 01, 01, 11, 00. The output variable, _z' is asserted when x1x2= 00 if and only if the three preceding pairs of inputs are x1x2= 01, 01 and 11, in that order.

2. Obtain a minimal state table for a clocked synchronous sequential network having a single input line _x' in which the symbols 0 and 1 are applied and a single output line _z'. An outputof 1 is to be produced if and only if the 3 input symbols following two consecutive input 0's consist of at least one 1. An example of input/output sequences that satisfy the conditions of the network specifications is:
   x=0100010010010010000000011
   z=0000001000000100000000001

3. Analyze the following clocked synchronous sequential network. Derive the next state and output equations. Obtain the excitation table, transition table, state table and state diagram.

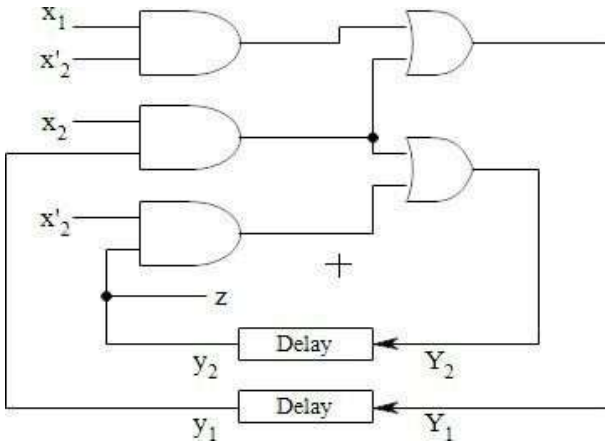


Course Outcome 2 (CO2): Analyze asynchronous sequential circuits

1. A reduced flow table for a fundamental-mode asynchronous sequential network is given below. Using the universal multiple-row state assignment, construct the corresponding expanded flow table and transition table. Assign outputs where necessary such that there is at most a single output change during the time the network is unstable. Assume that the inputs x1and x2 never change simultaneously.

Present state	Next state				Output (z)			
	Input state (x_1x_2)				Input state (x_1x_2)			
	00	01	10	11	00	01	10	11
A	A	B	A	D	1	-	0	-
B	D	B	B	C	-	0	1	-
C	A	C	C	C	-	1	1	0
D	D	C	A	D	0	-	-	1

2. Analyze the asynchronous sequential network by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in the fundamental mode with the restriction that only one input variable can change at a time.



3. Describe races in ASN with example.

Course Outcome 3 (CO3): Design hazard free circuits

1. Differentiate between static and dynamic hazard.
2. Examine the possibility of hazards in the (i) OR-AND logic circuit whose Boolean function is given by f = Σ(0,2,6,7) (ii) AND-OR logic circuit whose Boolean function is given by f = Σ(3,4,5,7) . Show how the hazard can be detected and eliminated in each circuit.
4. Investigate the problem of clock skew in practical sequential circuits and suggest solutions with justification to minimize or eliminate it.

Course Outcome 4 (CO4): Diagnose faults in digital circuits

1. Illustrate the fault table method used for effective test set generation for the circuit whose Boolean function is $z = x1‘x2 + x3$
2. Find the test vectors of all SA0 and SA1 faults of the circuit whose Boolean function is f = **x1’x2 + x1x2 x3** by the Kohavi algorithm.
3. Write a note on BIST techniques.

Course Outcome 5 (CO5): Analyze the role of HDLs in modeling and simulation of digital circuits in the VLSI design flow

1. Under stand the key considerations in different phases in VLSI design flow
2. Use HDLs for modeling and simulation of digital circuits.
3. Design HDL based FSM

SYLLABUS

Module 1:

Clocked Synchronous Networks Analysis of clocked Synchronous Sequential Networks (CSSN), Modeling of CSSN – State assignment and reduction, Design of CSSN, ASM Chart and its realization

Module 2:

Asynchronous Sequential Circuits Analysis of Asynchronous Sequential Circuits (ASC), Flow table reduction- Races in ASC, State assignment problem and the transition table-Design of AS, Design of ALU

Module 3:

Hazards – static and dynamic hazards – essential, Design of Hazard free circuits – Data synchronizers, Mixed operating mode asynchronous circuits, Practical issues- clock skew and jitter, Synchronous and asynchronous inputs – switch bouncing

Module 4:

Faults Fault table method – path sensitization method – Boolean difference method, Kohavi algorithm, Automatic test pattern generation – Built in Self-Test (BIST)

Module 5:

VLSI Design flow: Design entry: Schematic, FSM & HDL, different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling, Synthesis, simulation, VHDL constructs and codes for combinational and sequential circuits

Text Books

1. Donald G Givone, Digital Principles & Design, Tata McGraw Hill, 2003
2. John F Wakerly, Digital Design, Pearson Education, Delhi 2002

3. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning

4. M.Morris Mano and Michel.D.Ciletti, Digital Design with an introduction to HDL, VHDL and Verilog, Sixth edition Pearson education

Reference Books

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, Digital Systems Testing and Testable Design, John Wiley & Sons Inc.
2. Morris Mano, M.D.Ciletti, Digital Design, 5th Edition, PHI.
3. N. N. Biswas, Logic Design Theory, PHI
4. Richard E. Haskell, Darrin M. Hanna , Introduction to Digital Design Using Diligent FPGA Boards, LBE Books- LLC
5. Samuel C. Lee, Digital Circuits and Logic Design, PHI
6. Z. Kohavi, Switching and Finite Automata Theory, 2nd ed., 2001, TMH
7. R. Anand, Digital System Design Using VHDL, Khanna Book Publishing Company
8. Charles Roth, ―Digital System Design using VHDL, TMH, 2nd edition 2012.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Clocked Synchronous Networks**	
1.1	Analysis of clocked Synchronous Sequential Networks(CSSN)	2
1.2	Modelling of CSSN – State assignment and reduction	2
1.3	Design of CSSN	3
1.4	ASM Chart and its realization Mesh and Node Analysis	3
2	**Asynchronous Sequential Circuits**	
2.1	Analysis of Asynchronous Sequential Circuits (ASC)	2
2.2	Flow table reduction- Races in ASC	2
2.3	State assignment problem and the transition table- Design of AS	3
2.4	Design of ALU	3
3	**Hazards**	
3.1	Hazards – static and dynamic hazards – essential	1
3.2	Design of Hazard free circuits – Data synchronizers	1
3.3	Mixed operating mode asynchronous circuits	2
3.4	Practical issues- clock skew and jitter	1
3.5	Synchronous and asynchronous inputs – switch bouncing	2
4	**Faults**	
4.1	Fault table method – path sensitization method – Boolean difference method	2
4.2	Kohavi algorithm	2
4.3	Automatic test pattern generation – Built in Self Test(BIST)	2
5	**VLSI Design flow**	

5.1	Design entry: Schematic, FSM & HDL	3
5.2	different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling	3
5.3	Synthesis, simulation	2
5.4	VHDL constructs and codes for combinational and sequential circuits	4

Simulation Assignments:

At least one assignment should be design of digital circuits that can be used in day today life. This has to be done in a phased manner. The first phase involves the design in HDL (VHDL/ Verilog) and the second phase implementing the same in a hardware device. Some of the assignments are as listed below:

1. Design of vending machine
2. Design of ALU
3. Architecture of different FPGAs
4. Architecture of different CPLDs
5. Fault detection methods other than those mentioned in the syllabus
6. Metastability condition and methods to avoid it

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION,

Course Code: ECT312

Course: Digital System Design

Time: 3 hours **Max. Marks:100**

PART A

Answer ***all*** questions. Each question carries ***3 marks***.

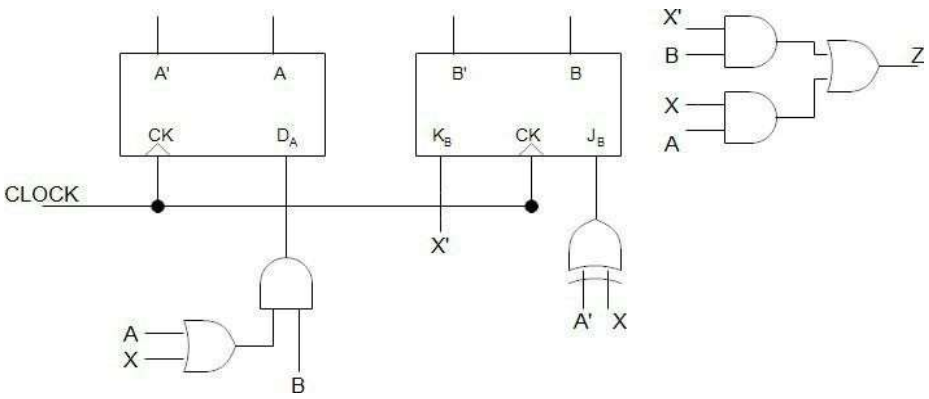
1. Differentiate Mealy and Moore models.
2. What are the elements in an ASM chart?
3. Describe one-hot assignment technique.
4. Define critical and non-critical races.
5. What is jitter? List the sources of clock jitter.
6. Differentiate positive skew and negative skew.
7. List the different types of faults in digital circuits.
8. Differentiate between fault and defect.
9. Mention the key considerations and steps involved in the design entry phase of a VLSI design flow.
10. How do HDLs facilitate the modeling and simulation of digital circuits in the VLSI design flow?

PART B

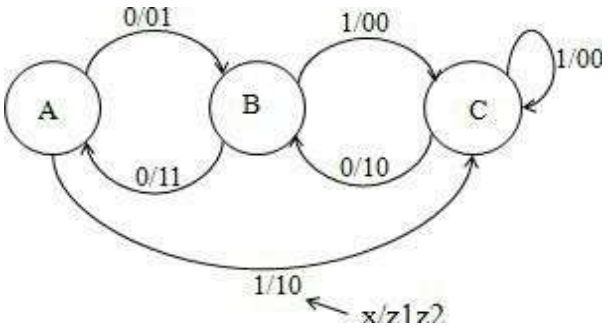
Answer one question from each module; each question carries 14 marks.

Module I

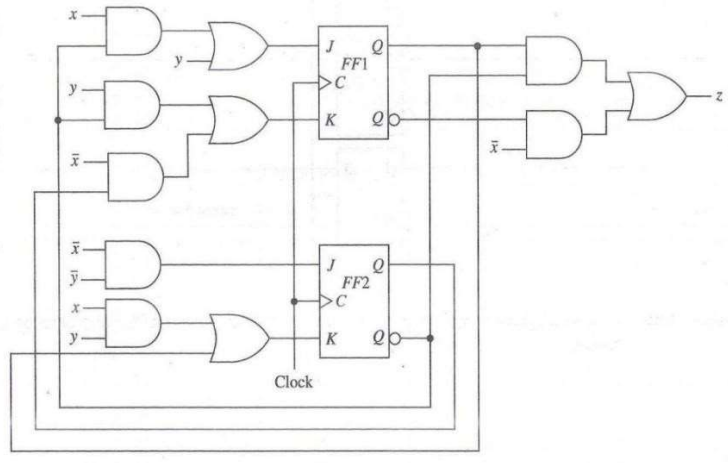
11. a) Analyze the following sequential network. Derive the next state and output equations. Obtain its transition table and state table. (8 marks)



b) Construct an ASM chart for the following state diagram shown. Determine the model of CSSN that this system conforms to with proper justification. (6 marks)



12. a) For the clocked synchronous sequential network, construct the excitation table, transition table, state table and state diagram. (8 marks)



b). Obtain a minimal state table for a clocked synchronous sequential network having a single input line ‗x' in which the symbols 0 and 1 are applied and a single output line ‗z'. Anoutput of 1 is to be produced if and only if the 3 input symbols following two consecutive

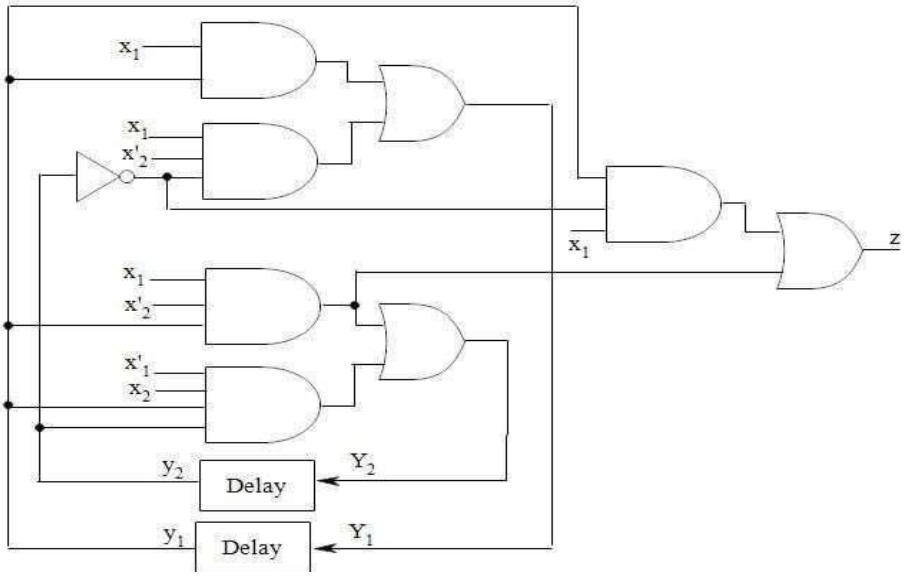
input 0's consist of at least one 1. An example of input/output sequences that satisfy the conditions of the network specifications is:

x= 0100010010010010000000011

z= 0000001000000100000000001 (6 marks)

Module – II

13. Analyze the asynchronous sequential network by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in the fundamental mode with the restriction that only one input variable can change at a time. (14 marks)



14. A reduced flow table for a fundamental-mode asynchronous sequential network is given below. Using the universal multiple-row state assignment, construct the corresponding expanded flow table and transition table. Assign outputs where necessary such that there is at most a single output change during the time the network is unstable. Assume that the inputs and never change simultaneously. (14 marks)

Present state	Next state				Output (z)			
	Input state (				Input state (			
	00	01	10	11	00	01	10	11
A	A	B	A	D	1	-	0	-
B	D	B	B	C	-	0	1	-
C	A	C	C	C	-	1	1	0
D	D	C	A	D	0	-	-	1

Module – III

15. a) Examine the possibility of hazard in the OR-AND logic circuit whose Boolean function is given by f = Σ(0,2,6,7). Show how the hazard can be detected and eliminated. (8 marks)

    b) Explain essential hazards in asynchronous sequential networks. What are the constraints to be satisfied to avoid essential hazards? (6 marks)

16. a) Draw the logic diagram of the POS expression Y= (x1+x2') (x2+x3). Show that there is a static-0 hazard when x1 and x3 are equal to 0 and x2 goes from 0 to 1. Find a way to remove the hazard by adding one or more gates. (9 marks)
    b) Discuss the concept of switch bouncing and suggest a suitable solution. (5 marks)

Module – IV

17. a) Illustrate the fault table method used for effective test set generation for the circuit whose Boolean function is $z = x_1'x_2 + x_3$ (8 marks)
    b) How can the timing problems in asynchronous sequential circuits be solved using mixed operating mode circuits? (6 marks)

18. a) Find the test vectors of all SA0 and SA1 faults of the circuit whose Boolean function is $f = x_1'x_2 + x_1x_2\ x_3$ by the Kohavi algorithm. (8 marks)
    b) Identify different test pattern generation for BIST (6 marks)

Module - V

19. a) What is a Finite State Machine (FSM) and how does it play a crucial role in VLSI design? How do you determine the number of states required for a specific application in the design of an FSM? (8 marks)
    b) How do you handle state encoding in the context of HDL-based FSM design, and what factors influence your choice of encoding? (6 marks)

20. a) Describe the principles of dataflow modeling in VHDL. How is dataflow modeling different from behavioral modeling? (7 marks)

    b) Discuss the use of component instantiation and configuration in structural modeling. How does it contribute to modularity in VHDL designs? (7 marks)

ECT206	COMPUTER ARCHITECTURE AND MICROCONTROLLERS	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to impart knowledge of basic computer architecture and modern microcontrollers.

Prerequisite: Logic Circuit Design

Course Outcomes: After the completion of the course the student will be able to

CO1	Explain the functional units, I/O and memory management w.r.t a typical computer architecture.
CO2	Distinguish between microprocessor and microcontroller.
CO3	Develop simple programs using assembly language programming.
CO4	Interface 8051 microcontroller with peripheral devices using ALP/Embedded C.
CO5	Familiarize system software and Advanced RISC Machine Architecture.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO1	3											3
CO2	3											3
CO3	3		3		3							3
CO4	3	3	3		3							3
CO5	3				3							3

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	10
Understand	20	20	20
Apply	20	20	70
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:
Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Course project : 15 marks

It is mandatory that a *course project* shall be undertaken by a student for this subject. The course project can be performed either as a hardware realization/simulation of a typical embedded system using Embedded C/ Assembly Language Programming. Instead of two assignments, two evaluations may be performed on the course project along with series tests, each carrying 5 marks. Upon successful completion of the project, a brief report shall be submitted by the studentwhich shall be evaluated for 5 marks. The report has to be submitted for academic auditing. A few sample course projects are listed below:

Sample Course Projects

The below mentioned projects shall be done with the help of IDE for 8051/ PIC /MSP /Arduino / Raspberry Pi-based interfacing boards/sensor modules.

1. Relay control
2. Distance measurement
3. Temperature measurement / Digital Thermometer
4. RF ID tags
5. Alphanumeric LCD display interface.
6. OLED display interfacing

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

SYLLABUS

Module 1: Computer Arithmetic and Processor Basics

Algorithms for binary multiplication and division. Fixed and floating-point number representation. Functional units of a computer, Von Neumann and Harvard computerarchitectures, CISC and RISC architectures. Processor Architecture – General internalarchitecture, Address bus, Data bus, control bus. Register set – status register, accumulator, program counter, stack pointer, general purpose registers. Processor operation – instructioncycle, instruction fetch, instruction decode, instruction execute, timing response, instruction sequencing and execution (basic concepts, datapath.

Module 2: 8051 Architecture

Microcontrollers and Embedded Processors. Architecture – Block diagram of 8051, Pin configuration, Registers, Internal Memory, Timers, Port Structures, Interrupts. Assembly Language Programming - Addressing Modes, Instruction set (Detailed study of 8051 instruction set is required).

Module 3: Programming and Interfacing of 8051

Simple programming examples in assembly language. Interfacing with 8051 using Assembly language programming: LED, Seven segment LED display. Programming in C - Declaring variables, Simple examples – delay generation, port programming, code conversion. Interfacing of – LCD display, Keyboard, Stepper Motor, DAC and ADC -- with 8051 and its programming.

Module 4: Advanced Concepts
8051 Timers/Counters - Modes and Applications. Serial Data Transfer – SFRs of serial port, working, Programming the 8051 to transfer data serially. Introduction to ARM – ARM family, ARM 7 register architecture. ARM programmer‘s model. System software -Assembler, Interpreter, Compiler, Linker, Loader, Debugger.

Module 5: The Memory System
Types of memory - RAM, ROM. Memory Characteristics and Hierarchy. Cache memory –The basics of Caches, Mapping techniques, Improving Cache performance. Virtual memory – Overlay, Memory management, Address translation. Input/ Output Organization – Introduction, Synchronous vs. asynchronous I/O, Programmed I/O, Interrupt driven I/O, Direct Memory Access.

Text Books

1. Muhammed Ali Mazidi & Janice Gilli Mazidi, R.D. Kinley, The 8051 microcontroller and Embedded System, Pearson Education, 2nd edition.
2. Subrata Ghoshal, Computer Architecture and Organization: From 8085 to Core2 Duo and beyond, Pearson, 2011.
3. Steve Furber, ARM System - on-chip Architecture, Pearson Education

Reference Books

1. Mano M M, Computer System Architecture, 3rd Ed, Prentice Hall of India.
2. Computer organization and design: The Hardware/Software interface/David A.Patterson, John L. Hennessy. — 5th ed.
3. Computer Organisation V. Carl Hamacher, Zvonko G. Vranesic, Safwat G.Zaky.
4. John P Hayes, Computer Architecture and Organization, McGraw Hill.
5. Ramesh S Goankar, 8085 Microprocessor Architecture, Applications and Programming, Penram International, 5/e.
6. The 8051 Microcontrollers: Architecture Programming and Applications, K Uma Rao & Andhe Pallavi, Pearson, 2011.
7. Stallings W., Computer Organisation and Architecture, 5/e, Pearson Education.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Computer Arithmetic and Processor Basics**	
1.1	Algorithms for binary multiplication and division	2
1.2	Fixed- and floating-point number representation in computers.	1
1.3	Functional units of a computer, Von Neumann and Harvard computer architectures, CISC and RISC architectures.	1
1.4	Processor Architecture – General internal architecture, Address bus, Data bus, control bus. Register set – status register, accumulator, program counter, stack pointer, general purpose registers.	2
1.5	Processor operation – instruction cycle, instruction fetch, instruction decode, instruction execute, timing response, instruction sequencing and execution (basic concepts), data path	3

2	**8051 Architecture**	
2.1	Microcontrollers and Embedded Processors and Applications	1
2.2	Architecture – Block diagram of 8051, Pin configuration, Registers, Internal Memory, Timers, Port Structures, Interrupts	3
2.3	Addressing Modes of 8051	1
2.4	Instruction sets (Detailed study of 8051 instructions)	4
3	**Programming and Interfacing of 8051**	
3.1	Simple programming examples in assembly language.	2
3.2	Interfacing programming in Assembly language	2
3.3	Programming in C - Declaring variables, Simple examples – delay generation, port programming, code conversion.	3
3.4	Interfacing of 7 segment LCD display	1
3.5	Interfacing of Keyboard and stepper motor	2
3.6	Interfacing of DAC and ADC	2
4	**Advanced Concepts**	
4.1	8051 Timers/Counters - Modes and Applications	2
4.2	Serial Data Transfer – SFRs of serial port, working, Programming the 8051 to transfer data serially	2
4.3	Introduction to ARM - ARM family, ARM 7 register architecture. ARM programmer‘s model	2
4.4	System software - Assembler, Interpreter, Compiler, Linker, Loader, Debugger.	2
5	**Memory System**	
5.1	Types of memory - RAM, ROM. Memory Characteristics and Hierarchy	2
5.2	Cache memory – The basics of Caches, Mapping techniques, Improving Cache performance	2
5.3	Virtual memory – Overlay, Memory management, Address translation	2
5.4	Input /Output Organization – Introduction, Synchronous vs. asynchronous I/O, Programmed I/O, Interrupt driven I/O, Direct Memory Access.	3

Simulation Assignments:

The following examples may be solved in C program

1. Program to convert the ASCII number into unpacked BCD.
2. Program to swap a number 0 x ab to 0 x ba, where a and b are hex digits.
3. Program to find the number of 1‘s in an 8-bit data item.
4. Program to display _M‘ and _E‘ on the LCD connected to 8051 using the BUSY FLAG.
5. Program to rotate a stepper motor 50_0 in the clock wise direction.
6. Program to toggle pin P1.4 every second using interrupts for a frequency of 22 MHz. Use timer 1 in mode 1.
7. Program to generate a square wave of 1 kHz with duty cycle 33%. Use timer 1 in interrupt mode with a crystal frequency of 11.0592 MHz.

Model Question paper
APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION,

Course Code:ECT206

Course: COMPUTER ARCHITECTURE AND MICROCONTROLLERS

Time: 3 hours **Max. Marks:100**

PART A

Answer ***all*** questions. Each question carries ***3 marks***.

1. Represent 4946.278941 as a 32 bit number in IEEE 754 format.
2. Which is more important for the functioning of a basic processor, Program Counter or Stack Pointer. Justify your answer.
3. List the components of 8051 microcontroller.
4. Write the operations happening in the following instructions:
   ADD A, 56
   XCHD A, @R1
   DJNZ R6, LABEL
   DIV AB
   XRL A, #0FFh
   JB P1.2 LABEL
5. Write an embedded C program for 8051 microcontroller to continuously rotate a stepper motor clockwise.
6. Write an embedded C program for 8051 microcontroller to blink P2.5 every 2 seconds.
7. List the different modes and give corresponding uses of timers in 8051 microcontroller.
8. Which are the SFRs used for serial communication in 8051 microcontroller. Give there functions.
9. Illustrate the memory hierarchy in a computer system.
10. Is ROM a random access memory? Justify your answer.

PART B

Answer one question each from all modules

Module 1

11. a) With an example explain the ‒shift and add‖ algorithm for multiplying two binary numbers. (5 marks)
    b) With relevant diagrams illustrate the functioning of a basic (non – pipelined) processor. (9 marks)

12. a) Differentiate RISC and CISC architectures. (4 marks)
    b) Explain Instruction Cycle with a sample timing diagram (10 marks)

Module 2

13. a) Illustrate the complete memory organization of 8051 microcontroller (10 marks)
    b) Differentiate microprocessors and microcontrollers. (4 marks)

14. a) Explain about the Addressing Modes of 8051 microcontroller with examples. (7 marks)
    b) Describe the classification of the Instruction Set of 8051 microcontroller with examples. (7 marks)

Module 3

15. a) Write an embedded C program for 8051 microcontroller to read an analogue signal from an ADC and reproduce the same using a DAC (9 marks)
    b) Write an assembly language program for 8051 microcontroller to sort N number in ascending order. Assume that the numbers are stored in continuous locations starting from 0x4321 onwards. (5 marks)

16. a) Write an embedded C program for 8051 microcontroller to repeatedly display the sequence 1,5,8,0,2,6,4,9,3,7 using a 7 – segment display with a delay of 1.5 seconds betweeneach number. (9 marks)
b) Write an assembly language program for 8051 microcontroller to find the cube of an 8 –bit number (5 marks)

Module 4

17. a) Assume a switch is connected to pin PL7. Write a embedded C program for 8051 microcontroller to monitor its status and send two messages to serial port continuously as follows:
    SW=0 send –NO‖
    SW=1 send –YES‖
    Assume XTAL = 11.0592 MHz, 9600 baud, 8-bit data, and 1 stop bit. (10 marks)
    b) Describe the ARM 7 register architecture (4 marks)

18. a)Write a embedded C program for 8051 microcontroller to send the message –Hello World!‖ to serial port. Assume a SW is connected to pin P1.2. Monitor its status and set the baud rate as follows:
    SW = 0 , 4800 baud rate
    SW = 1 , 9600 baud rate
    Assume XTAL = 11.0592 Mhz, 8 – bit data, and 1 stop bit (10 marks)
    b) Explain how a HLL program is executed as machine language in a processor (4 marks)

Module 5

19. a) Differentiate synchronous and asynchronous I/O. Which is more efficient with respect to processor utilization? Justify your answer. (8 marks)
    b) Explain direct mapping of cache memory with an example (6 marks)

20. a) Differentiate interrupt driven and programmed I/O. Which is more efficient with respect to processor utilization? Justify your answer (8 marks)

b) Explain about memory management using virtual memory. (6 marks)

ECL202	**ANALOG CIRCUITS AND SIMULATION LAB**	**CATEGORY**	**L**	**T**	**P**	**CREDIT**
		PCC	0	0	3	2

Preamble: This course aims to

(i) Familiarize students with the Analog Circuits Design through the implementation of basic Analog Circuits using discrete components.

(ii) Familiarize students with simulation of basic Analog Circuits.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO1	Design and demonstrate the functioning of basic analog circuits using discrete components.
CO2	Design and simulate the functioning of basic analog circuits using simulation tools.
CO3	Function effectively as an individual and in a team to accomplish the given task.

Mapping of course outcomes with program outcomes

	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO12**
CO1	3	3	3						2			2
CO2	3	3	3		3				2			2
CO3	3	3	3						3			3

Assessment Pattern

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
150	75	75	2.5Hrs

Continuous Internal Evaluation Pattern:

Attribute	Mark
Attendance	15
Continuous assessment	30
Internal Test (Immediately before the second series test)	30

End Semester Examination Pattern: The following guidelines should be followed regarding award of marks.

Attribute	Mark
Preliminary work	15
Implementing the work/Conducting the experiment	10
Performance, result and inference (usage of equipments and trouble shooting)	25
Viva voce	20
Record	5

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

List of Experiments:

Part A : List of Experiments using discrete components [Any Six experiments mandatory]

1. RC integrating and differentiating circuits (Transient analysis with different inputs and frequency response)
2. Clipping and clamping circuits (Transients and transfer characteristics)
3. RC coupled CE amplifier - frequency response characteristics
4. MOSFET amplifier (CS) - frequency response characteristics
5. Cascade amplifier – gain and frequency response
6. Cascode amplifier -frequency response
7. Feedback amplifiers (current series, voltage series) - gain and frequency response
8. Low frequency oscillators –RC phase shift or Wien bridge
9. Power amplifiers (transformer less) - Class B and Class AB
10. Transistor series voltage regulator (load and line regulation)

PART B: Simulation experiments [Any Six experiments mandatory]

The experiments shall be conducted using open tools such as QUCS, KiCad or variants of SPICE.

1. RC integrating and differentiating circuits (Transient analysis with different inputs and frequency response)
2. Clipping and clamping circuits (Transients and transfer characteristics)
3. RC coupled CE amplifier - frequency response characteristics
4. MOSFET amplifier (CS) - frequency response characteristics
5. Cascade amplifier – gain and frequency response
6. Cascode amplifier – frequency response
7. Feedback amplifiers (current series, voltage series) - gain and frequency response
8. Low frequency oscillators – RC phase shift or Wien Bridge
9. Power amplifiers (transformer less) - Class B and Class AB
10. Transistor series voltage regulator (load and line regulation)

ECL204	**MICROCONTROLLER LAB**	**CATEGORY**	**L**	**T**	**P**	**CREDIT**
		PCC	0	0	3	2

Preamble:

This course aims to
(i) Familiarize the students with Assembly Language Programming of modern microcontrollers.
(ii) Impart the skills for interfacing the microcontroller with the help of Embedded C/Assembly Language Programming.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO1	Write an Assembly language program/Embedded C program for performing data Manipulation.
CO2	Apply an industry compatible hardware description language to implement digital circuits
CO3	Implement digital circuis on FPGA boards and connect external hardware to the boards
CO4	**CO 2** Develop ALP/Embedded C Programs to interface microcontroller with peripherals **CO 3** Perform programming/interfacing experiments with IDE for modern microcontrollers.Function effectively as an individual and in a team to accomplish the given task

Mapping of course outcomes with program outcomes

	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO12**
CO1	3	3	3						3			3
CO2	3	1	1	3	3				3			3
CO3	3	1	1	3	3				3	1		3
CO4	3	3	3		3				3			3

Assessment Pattern

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
150	75	75	2.5Hrs

Continuous Internal Evaluation Pattern:

Attribute	Mark
Attendance	15
Continuous assessment	30
Internal Test (Immediately before the second series test)	30

End Semester Examination Pattern: The following guidelines should be followed regarding award of marks.

Attribute	Mark
Preliminary work	15
Implementing the work/Conducting the experiment	10
Performance, result and inference (usage of equipments and trouble shooting)	25
Viva voce	20
Record	5

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Level Assessment Questions

Course Outcome 1 (CO1): Design and Development of combinational circuits

1. Design a one bit full adder using gates and implement and test it on board.
2. Implement and test the logic function f(A,B,C)=∑m(0,1,3,6) using an 8:1 Mux IC
3. Convert a D flip-flop to T flip-flop and implement and test on board.

Course Outcome 2 and 3 (CO2 and CO3): Implementation of logic circuits on tiny FPGA

1. Design and implement a one bit subtracter in Verilog and implement and test it on a tiny FPGA board.
2. Design and implement a J-K flip-flop in Verilog, implement and test it on a tiny FPGA board.
3. Design a 4:1 Multiplexer in Verilog and implement and test it on tiny FPGA board.

List of Experiments:

It is compulsory to conduct a minimum of 5 experiments from Part A and a minimum of 5 experiments from Part B.

Part A (Any 5)

The following experiments can be conducted on breadboard or trainer kits.

1. Realization of functions using basic and universal gates (SOP and POS forms).
2. Design and Realization of half /full adder and subtractor using basic gates and universal gates.
3. 4 bit adder/subtractor and BCD adder using 7483.
4. Study of Flip Flops: S-R, D, T, JK and Master Slave JK FF using NAND gates.
5. Asynchronous Counter:3 bit up/down counter
6. Asynchronous Counter:Realization of Mod N counter
7. Synchronous Counter: Realization of 4-bit up/down counter.
8. Synchronous Counter: Realization of Mod-N counters.
9. Ring counter and Johnson Counter. (using FF & 7495).
10. Realization of counters using IC‘s (7490, 7492, 7493).
11. Multiplexers and De-multiplexers using gates and ICs. (74150, 74154)
12. Realization of combinational circuits using MUX & DEMUX.
13. Random Sequence generator using LFSR.

PART B (Any 5)

The following experiments aim at training the students in digital circuit design with verilog and Implementation in small FPGAs. Small, low cost FPGAs, that can be driven by open tools for simulation, synthesis and place and route, such as Tiny FPGA or Lattice iCEstick can be used. Open software tools such as yosis (for simulation and synthesis) and arachne (for place and route) may be used. The experiments will lay the foundation for digital design with FPGA with the objective of increased employability.

Experiment 1. Realization of Logic Gates and Familiarization of FPGAs

(a) Familiarization of a small FPGA bboard and its ports and interface.

(b) Create the .pcf files for your FPGA board.

(c) Familiarization of the basic syntax of verilog

(d) Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables.

(e) Verify the universality and non associativity of NAND and NOR gates by uploading the corresponding verilog files to the FPGA boards.

Experiment 2: Adders in Verilog

(a) Development of verilog modules for half adder in 3 modeling styles (dataflow/structural/ behavioral).

(b) Development of verilog modules for full adder in structural modeling using half adder.

Experiment 3: Mux and Demux in Verilog

(a) Development of verilog modules for a 4x1 MUX.

(b) Development of verilog modules for a 1x4 DEMUX.

Experiment 4: Flipflops and counters

(a) Development of verilog modules for SR, JK and D flipflops.

(b) Development of verilog modules for a binary decade/Johnson/Ring counters

Experiment 5. Multiplexer and Logic Implementation in FPGA

(a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality.

(b) Use the above module to realize the logic function f (A, B, C) = ∑m(0, 1, 3, 7) and test it.

(c) Use the same 8 : 1 multiplexer to realize the logic function f (A, B, C, D) = ∑m(0, 1, 3, 7, 10, 12) by partitioning the truth table properly and test it.

Experiment 6: Flip-Flops and their Conversion in FPGA

(a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board.

(b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D

Experiment 7: Asynchronous and Synchronous Counters in FPGA

(a) Make a design of a 4-bit up down ripple counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board.

(b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board.

Experiment 8: Universal Shift Register in FPGA

(a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board.

(b) Implement ring and Johnson counters with it.

Experiment 9. BCD to Seven Segment Decoder in FPGA

(a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality.

(b) Test it with switches and seven segment display. Use ouput ports for connection to the display.