SEMESTER 3

ELECTRONICS ENGINEERING

(VLSI Design and Technology)

SEMESTER S3

MATHEMATICS FOR ELECTRICAL SCIENCE AND PHYSICAL SCIENCE – 3

(Common to B & C Groups)

Course Code	**GYMAT301**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Basic knowledge in complex numbers.	**Course Type**	Theory

Course Objectives:

1. To introduce the concept and applications of Fourier transforms in various engineering fields.
2. To introduce the basic theory of functions of a complex variable, including residue integration and conformal transformation, and their applications

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Fourier Integral, From Fourier series to Fourier Integral, Fourier Cosine and Sine integrals, Fourier Cosine and Sine Transform, Linearity, Transforms of Derivatives, Fourier Transform and its inverse, Linearity, Transforms of Derivative. **(Text 1: Relevant topics from sections 11.7, 11.8, 11.9)**	**9**
2	Complex Function, Limit, Continuity, Derivative, Analytic functions, Cauchy-Riemann Equations (without proof), Laplace's Equations, Harmonic functions, Finding harmonic conjugate, Conformal mapping, Mappings of $w= z^2,\ w=e^z, w=\frac{1}{z},\ w= sinz$. **(Text 1: Relevant topics from sections 13.3, 13.4, 17.1, 17.2, 17.4)**	**9**
3	Complex Integration: Line integrals in the complex plane (Definition & Basic properties), First evaluation method, Second evaluation method, Cauchy's integral theorem (without proof) on simply connected domain,	**9**

	Independence of path, Cauchy integral theorem on multiply connected domain (without proof), Cauchy Integral formula (without proof). **(Text 1: Relevant topics from sections 14.1, 14.2, 14.3)**	
4	Taylor series and Maclaurin series, Laurent series (without proof), Singularities and Zeros – Isolated Singularity, Poles, Essential Singularities, Removable singularities, Zeros of Analytic functions – Poles and Zeros, Formulas for Residues, Residue theorem (without proof), Residue Integration- Integral of Rational Functions of $cos\theta$ and $sin\theta$. **(Text 1: Relevant topics from sections 15.4, 16.1, 16.2, 16.3, 16.4)**	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Determine the Fourier transforms of functions and apply them to solve problems arising in engineering.	**K3**
CO2	Understand the analyticity of complex functions and apply it in conformal mapping.	**K3**
CO3	Compute complex integrals using Cauchy's integral theorem and Cauchy's integral formula.	**K3**
CO4	Understand the series expansion of complex function about a singularity and apply residue theorem to compute real integrals.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**
CO2	**3**	**3**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**
CO3	**3**	**3**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**
CO4	**3**	**3**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Advanced Engineering Mathematics	Erwin Kreyszig	John Wiley & Sons	10^{th} edition, 2016

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Complex Analysis	Dennis G. Zill, Patrick D. Shanahan	Jones & Bartlett	3^{rd} edition, 2015
2	Higher Engineering Mathematics	B. V. Ramana	McGraw-Hill Education	39^{th} edition, 2023
3	Higher Engineering Mathematics	B.S. Grewal	Khanna Publishers	44^{th} edition, 2018
4	Fast Fourier Transform - Algorithms and Applications	K.R. Rao, Do Nyeon Kim, Jae Jeong Hwang	Springer	1^{st} edition, 2011

SEMESTER S3

SOLID STATE DEVICES

Course Code	**PCECT302**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Physics of Electrical Science (GBPHT121)	**Course Type**	Theory

Course Objectives:

1. This course explains the physical processes and working principles of semiconductor devices, while relating the device performance to material parameters and design criteria.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Review of Semiconductor physics:** Equilibrium and steady state conditions, Concept of effective mass and Fermi level, Density of states & Effective density of states, Equilibrium concentration of electrons and holes. **Excess carriers in semiconductors:** Generation and recombination mechanisms of excess carriers, quasi-Fermi levels. **Carrier transport in semiconductors**: Drift, conductivity and mobility, variation of mobility with temperature and doping, Hall Effect. Diffusion, Einstein relations, Poisson equations, Continuity equations, Current flow equations, Diffusion length, Gradient of quasi-Fermi level.	**13**
2	**PN junctions**: Contact potential, Electrical Field, Potential and Charge distribution at the junction, Biasing and Energy band diagrams, Ideal diode equation. **Bipolar junction transistor**: Transistor action, Base width	**12**

	modulation, Current components in a BJT, Derivation of current components.	
3	**Metal Semiconductor contacts**: Electron affinity and work function, Ohmic and Rectifying Contacts, current voltage characteristics. **Ideal MOS capacitor**: band diagrams at equilibrium, accumulation, depletion and inversion, surface potential, CV characteristics, effects of real surfaces, threshold voltage, body effect. **MOSFET**- Drain current equation of enhancement type MOSFET (derivation)- linear and saturation region, Drain characteristics, transfer characteristics.	**11**
4	**MOSFET scaling**: Need for scaling, constant voltage scaling and constant field scaling. Sub- threshold conduction in MOS. **Short channel effects in MOSFETs**: Channel length modulation, Drain Induced Barrier Lowering, Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects. **MESFET and FinFET**: Structure, operation and advantages.	**8**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply Fermi-Dirac statistics to compare equilibrium carrier concentration.	**K3**
CO2	State different carrier transport mechanisms in extrinsic semiconductors and obtain the current densities due to this transport.	**K3**
CO3	Apply the concept of semiconductor physics to solve the current components in semiconductor devices.	**K3**
CO4	Analyze the response of semiconductor devices for different biasing conditions	**K3**
CO5	Outline the effects of scaling in semiconductor devices.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**											
CO2	**3**	**2**										
CO3	**3**	**2**										**2**
CO4	**3**	**2**	**2**									**2**
CO5	**3**	**2**	**2**									**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Semiconductor Physics and Devices	Neamen	McGraw Hill	4/e, 2017
2	Physics of Semiconductor Devices	Sze S.M	John Wiley	3/e, 2015
3	Semiconductor Devices: Physics and Technology	Sze S.M	John Wiley	3/e, 2016
4	Operation and Modelling of the MOS Transistor	Yannis Tsividis	Oxford University Press	3/e,2010

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117106091
2	https://nptel.ac.in/courses/117106091
3	https://nptel.ac.in/courses/117106091
4	https://nptel.ac.in/courses/117106091

SEMESTER S3

ANALOG CIRCUITS

Course Code	**PCECT303**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	BEE/(GYEST104)	**Course Type**	Theory

Course Objectives:

1. By the end of this course, students will be able to design and analyze various analog circuits, including wave shaping circuits, amplifiers, oscillators, and voltage regulators.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Wave Shaping Circuits:** RC differentiating and integrating circuits, Analysis of First order RC low pass and high pass filter for step input -rise time, band width. Diode Clipping and clamping circuits. **BJT/MOSFET Biasing:** Need for biasing, DC load line, operating point, BJT biasing (CE configuration)– fixed bias & voltage divider bias (Design & analysis). MOSFET biasing,	**10**
2	**BJT Amplifiers:** Design of RC coupled CE amplifier - Small signal analysis of CE amplifier using hybrid-π model (low and mid frequency`). The high-frequency hybrid-π model of BJT, Miller effect, High frequency response of single stage CE amplifier, short circuit current gain, cut-off frequency f_β & unity gain bandwidth f_T . **MOSFET Amplifiers:** Design of CS amplifier, Small signal analysis using hybrid-π model (mid frequency only), Small signal voltage gain, input & output impedance, CS stage with current source load and diode connected load. **Multistage BJT Amplifiers:** Types of multistage amplifiers, Effect of cascading on gain and bandwidth.	**12**

	Small signal voltage gain, input & output impedance of BJT cascode amplifier using hybrid-π model.	
3	**Feedback amplifiers:** The general feedback structure, Effect of negative feedback on gain, bandwidth, noise reduction and distortion. The four basic feedback topologies, Analysis of discrete BJT circuits in voltage-series and voltage-shunt feedback topologies - voltage gain, input and output impedance. **Oscillators:** Classification, criterion for oscillation, Wien bridge oscillator, Hartley and Crystal oscillator. (working principle and design equations of the circuits; analysis of Wien bridge oscillator only required).	**11**
4	**Power amplifiers:** Classification, Transformer coupled class A power amplifier, push pull class B and class AB power amplifiers, complementary-symmetry class B and Class AB power amplifiers, class C and D power amplifier - efficiency and distortion (no analysis required) **Linear Voltage Regulators:** Types of voltage regulators- series and shunt - working and design, load & line regulation, short circuit protection and fold back protection.	**11**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design wave shaping circuits using first order RC network and diodes.	**K3**
CO2	Analyze single stage and multistage BJT amplifier circuits using equivalent models.	**K3**
CO3	Apply the principles of feedback in the design of oscillators.	**K3**
CO4	Design power amplifiers and voltage regulator circuits.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2		2							2
CO2	3	3			2							2
CO3	3	3	`2		2							2
CO4	3	3	2		2							2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Electronic Devices and Circuit Theory.	Robert Boylestad and L Nashelsky	Pearson	11th edition, 2015
2	Microelectronic Circuits	Sedra A. S. and K. C. Smith,	Oxford University Press, 2013	6th edition, 2013
3	Electronic Circuits and Devices	Theodore F. Bogart; Beasley, Jeffrey S.; Guillermo Rico	Pearson Education India	6th edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of Microelectronics	Razavi B.	Wiley	2nd edition, 2015
2	Electronic Devices and Circuits	David A Bell	Oxford University Press	5th edition, 2008
3	Electronic Circuits Analysis and Design 1	D. Meganathan	Yes Dee Publishing	1st edition, 2023
4	Analysis and Design of Electronic Circuits	K. Gopakumar	OWL Books	1st edition, 2023

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/108/106/108106188/
2	https://archive.nptel.ac.in/courses/108/106/108106188/
3	https://archive.nptel.ac.in/courses/108/106/108106188/

SEMESTER S3

LOGIC CIRCUIT DESIGN

(Common to EC and AE Branches)

Course Code	**PBECT304**	**CIE Marks**	60
Teaching Hours/Week (L: T:P: R)	3:0:0:1	**ESE Marks**	40
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	GYEST104 Introduction to Electrical & Electronics Engineering	**Course Type**	Theory

Course Objectives:

1. To understand the number systems in digital systems.
2. To introduce the basic postulates of Boolean algebra, digital logic gates and Boolean expressions
3. To design and implement combinational and sequential circuits.
4. To design and implement digital circuits using Hardware Descriptive Language like Verilog on FPGA.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to digital circuits:** Review of number systems representation-conversions, Arithmetic of Binary number systems, Signed and unsigned numbers, BCD. **Boolean algebra:** Theorems, sum of product and product of sum - simplification, canonical forms- min term and max term, Simplification of Boolean expressions - Karnaugh map (upto 4 variables), Implementation of Boolean expressions using universal gates.	9
2	**Combinational logic circuits**- Half adder and Full adders, Subtractors, BCD adder, Ripple carry and carry look ahead adders, Decoders, Encoders, Code converters, Comparators, Parity generator, Multiplexers, De-multiplexers, Implementation of Boolean algebra using MUX. Introduction to Verilog HDL – Basic language elements, Basic implementation of logic gates and combinational circuits.	9

3	**Sequential Circuits:** SR Latch, Flip flops - SR, JK, Master-Slave JK, D and T Flip flops. Conversion of Flip flops, Excitation table and characteristic equation. Shift registers-SIPO, SISO, PISO, PIPO and Universal shift registers. Ring and Johnsons counters. Design of Asynchronous, Synchronous and Mod N counters.	**9**
4	**Finite state machines** - Mealy and Moore models, State graphs, State assignment, State table, State reduction. **Logic Families:** -Electrical characteristics of logic gates (Noise margin, Fan-in, Fan-out, Propagation delay, Transition time, Power -delay product) -TTL, ECL, CMOS. Circuit description and working of TTL and CMOS inverter, CMOS NAND and CMOS NOR gates.	**9**

Suggestion on Project Topics

- A random sequence generator
- Traffic light controller
- Multiplexer based person priority check in system at airport
- Waveform generator
- Object/Visitor counter
- Fast adders
- Hamming code-based parity checker
- Arithmetic Logic Unit using FPGA

Course Assessment Method
(CIE: 60 marks, ESE: 40 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**30**	**12.5**	**12.5**	**60**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 2 marks **(8x2 =16marks)**	• Each question carries 6 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 2 sub divisions. **(4x6 = 24 marks)**	**40**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply the knowledge of digital representation of information and Boolean algebra to deduce optimal digital circuits.	**K3**
CO2	Design and implement combinational logic circuits, sequential logic circuits and finite state machines.	**K5**
CO3	Design and implement digital circuits on FPGA using hardware description language (HDL).	**K5**
CO4	Outline the performance of logic families with respect to different parameters.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2								3
CO2	3	3	3	3	3	3	3	3	3			3
CO3	3	3	3	3	3	3	3	3	3	3	3	3
CO4	3		2									3

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Fundamentals	Thomas L. Floyd	Pearson Education	11th Edition, 2017
2	Fundamentals of Digital Logic with Verilog Design	Stephen Brown	McGraw Hill Education	2nd Edition
3	Fundamentals of Logic Design	Roth C.H	Jaico Publishers. V Ed., 2009.	6th Edition, 2009
4	Modern digital Electronics	R.P. Jain	Tata McGraw Hill, 2009	4th Edition, 2009

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog	M Morris Mano, Michael D. Ciletti	Pearson India	6th Edition, 2018
2	Fundamentals of Digital Circuits	A. Ananthakumar	PHI	4th Edition, 2016
3	Introduction to Logic Circuits & Logic Design with Verilog	Brock J. LaMeres	Springer	2nd Edition, 2019
4	Digital Design Verilog HDL and Fundamentals	Joseph Cavanagh	CRC Press	1st Edition, 2008
5	Digital Circuits and Systems	D.V. Hall	Tata McGraw Hill	1989

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/
2	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/
3	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/
4	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/

PBL Course Elements

L: Lecture (3 Hrs.)	R: Project (1 Hr.), 2 Faculty Members		
	Tutorial	**Practical**	**Presentation**
Lecture delivery	Project identification	Simulation/ Laboratory Work/ Workshops	Presentation (Progress and Final Presentations)
Group discussion	Project Analysis	Data Collection	Evaluation
Question answer Sessions/ Brainstorming Sessions	Analytical thinking and self-learning	Testing	Project Milestone Reviews, Feedback, Project reformation (If required)
Guest Speakers (Industry Experts)	Case Study/ Field Survey Report	Prototyping	Poster Presentation / Video Presentation: Students present their results in a 2 to 5 minutes video

Assessment and Evaluation for Project Activity

Sl. No	Evaluation for	Allotted Marks
1	Project Planning and Proposal	**5**
2	Contribution in Progress Presentations and Question Answer Sessions	**4**
3	Involvement in the project work and Team Work	**3**
4	Execution and Implementation	**10**
5	Final Presentations	**5**
6	Project Quality, Innovation and Creativity	**3**
Total		**30**

Project Assessment and Evaluation criteria (30 Marks)

1. **Project Planning and Proposal (5 Marks)**

   - Clarity and feasibility of the project plan
   - Research and background understanding
   - Defined objectives and methodology

2. **Contribution in Progress Presentation and Question Answer Sessions (4 Marks)**

   - Individual contribution to the presentation
   - Effectiveness in answering questions and handling feedback

3. **Involvement in the Project Work and Team Work (3 Marks)**

   - Active participation and individual contribution

- Teamwork and collaboration

4. Execution and Implementation (10 Marks)

- Adherence to the project timeline and milestones
- Application of theoretical knowledge and problem-solving
- Final Result

5. Final Presentation (5 Marks)

- Quality and clarity of the overall presentation
- Individual contribution to the presentation
- Effectiveness in answering questions

6. Project Quality, Innovation, and Creativity (3 Marks)

- Overall quality and technical excellence of the project
- Innovation and originality in the project
- Creativity in solutions and approaches

SEMESTER S3

INTRODUCTION TO ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

Course Code	**GNEST305**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Demonstrate a solid understanding of advanced linear algebra concepts, machine learning algorithms and statistical analysis techniques relevant to engineering applications, principles and algorithms.
2. Apply theoretical concepts to solve practical engineering problems, analyze data to extract meaningful insights, and implement appropriate mathematical and computational techniques for AI and data science applications.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to AI and Machine Learning**: Basics of Machine Learning - types of Machine Learning systems-challenges in ML- Supervised learning model example- regression models- Classification model example- Logistic regression-unsupervised model example- K-means clustering. Artificial Neural Network- Perceptron- Universal Approximation Theorem (statement only)- Multi-Layer Perceptron- Deep Neural Network- demonstration of regression and classification problems using MLP.(Text-2)	11
2	**Mathematical Foundations of AI and Data science**: Role of linear algebra in Data representation and analysis – Matrix decomposition- Singular Value Decomposition (SVD)- Spectral decomposition- Dimensionality reduction technique-Principal Component Analysis (PCA). (Text-1)	11
3	**Applied Probability and Statistics for AI and Data Science**: Basics of probability-random variables and statistical measures - rules in probability-	11

	Bayes theorem and its applications- statistical estimation-Maximum Likelihood Estimator (MLE) - statistical summaries- Correlation analysis- linear correlation (direct problems only)- regression analysis- linear regression (using least square method) (Text book 4)	
4	**Basics of Data Science**: Benefits of data science-use of statistics and Machine Learning in Data Science- data science process - applications of Machine Learning in Data Science- modelling process- demonstration of ML applications in data science- Big Data and Data Science. (For visualization the software tools like Tableau, PowerBI, R or Python can be used. For Machine Learning implementation, Python, MATLAB or R can be used.)(Text book-5)	**11**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply the concept of machine learning algorithms including neural networks and supervised/unsupervised learning techniques for engineering applications.	**K3**
CO2	Apply advanced mathematical concepts such as matrix operations, singular values, and principal component analysis to analyze and solve engineering problems**.**	**K3**
CO3	Analyze and interpret data using statistical methods including descriptive statistics, correlation, and regression analysis to derive meaningful insights and make informed decisions.	**K3**
CO4	Integrate statistical approaches and machine learning techniques to ensure practically feasible solutions in engineering contexts.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	3	3								
CO2	3	3	3	3								
CO3	3	3	3	3								
CO4	3	3	3	3								
CO5	3	3	3	3								

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introduction to Linear Algebra	Gilbert Strang	Wellesley-Cambridge Press	6th edition, 2023
2	Hands-on machine learning with Scikit-Learn, Keras, and TensorFlow	Aurélien Géron	O'Reilly Media, Inc.	2nd edition,2022
3	Mathematics for machine learning	Deisenroth, Marc Peter, A. Aldo Faisal, and Cheng Soon Ong	Cambridge University Press	1st edition. 2020
4	Fundamentals of mathematical statistics	Gupta, S. C., and V. K. Kapoor	Sultan Chand & Sons	9th edition, 2020
5	Introducing data science: big data, machine learning, and more, using Python tools	Cielen, Davy, and Arno Meysman	Simon and Schuster	1st edition, 2016

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Data science: concepts and practice	Kotu, Vijay, and Bala Deshpande	Morgan Kaufmann	2nd edition, 2018
2	Probability and Statistics for Data Science	Carlos Fernandez-Granda	Center for Data Science in NYU	1st edition, 2017
3	Foundations of Data Science	Avrim Blum, John Hopcroft, and Ravi Kannan	Cambridge University Press	1st edition, 2020
4	Statistics For Data Science	James D. Miller	Packt Publishing	1st edition, 2019
5	Probability and Statistics - The Science of Uncertainty	Michael J. Evans and Jeffrey S. Rosenthal	University of Toronto	1st edition, 2009
6	An Introduction to the Science of Statistics: From Theory to Implementation	Joseph C. Watkins	chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.math.arizo	Preliminary Edition.

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/106/106/106106198/
2	https://archive.nptel.ac.in/courses/106/106/106106198/ https://ocw.mit.edu/courses/18-06-linear-algebra-spring-2010/resources/lecture-29-singular-value-decomposition/
3	https://ocw.mit.edu/courses/18-650-statistics-for-applications-fall-2016/resources/lecture-19-video/
4	https://archive.nptel.ac.in/courses/106/106/106106198/

SEMESTER S3/S4

ECONOMICS FOR ENGINEERS

(Common to All Branches)

Course Code	UCHUT346	CIE Marks	50
Teaching Hours/Week (L: T:P: R)	2:0:0:0	ESE Marks	50
Credits	2	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. Understanding of finance and costing for engineering operation, budgetary planning and control
2. Provide fundamental concept of micro and macroeconomics related to engineering industry
3. Deliver the basic concepts of Value Engineering.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Basic Economics Concepts - Basic economic problems – Production Possibility Curve – Utility – Law of diminishing marginal utility – Law of Demand - Law of supply – Elasticity - measurement of elasticity and its applications – Equilibrium- Changes in demand and supply and its effects Production function - Law of variable proportion – Economies of Scale – Internal and External Economies – Cobb-Douglas Production Function	6
2	Cost concepts – Social cost, private cost – Explicit and implicit cost – Sunk cost - Opportunity cost - short run cost curves - Revenue concepts Firms and their objectives – Types of firms – Markets - Perfect Competition – Monopoly - Monopolistic Competition - Oligopoly (features and equilibrium of a firm)	6
3	Monetary System – Money – Functions - Central Banking –Inflation - Causes and Effects – Measures to Control Inflation - Monetary and Fiscal	6

	policies – Deflation Taxation – Direct and Indirect taxes (merits and demerits) - GST National income – Concepts - Circular Flow – Methods of Estimation and Difficulties - Stock Market – Functions- Problems faced by the Indian stock market-Demat Account and Trading Account – Stock market Indicators- SENSEX and NIFTY	
4	Value Analysis and value Engineering - Cost Value, Exchange Value, Use Value, Esteem Value - Aims, Advantages and Application areas of Value Engineering - Value Engineering Procedure - Break-even Analysis - Cost-Benefit Analysis - Capital Budgeting - Process planning	**6**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/Case study / Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
10	**15**	**12.5**	**12.5**	**50**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• Minimum 1 and Maximum 2 Questions from each module. • Total of 6 Questions, each carrying 3 marks **(6x3 =18marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 2 sub divisions. Each question carries 8 marks. **(4x8 = 32 marks)**	**50**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the fundamentals of various economic issues using laws and learn the concepts of demand, supply, elasticity and production function.	**K2**
CO2	Develop decision making capability by applying concepts relating to costs and revenue, and acquire knowledge regarding the functioning of firms in different market situations.	**K3**
CO3	Outline the macroeconomic principles of monetary and fiscal systems, national income and stock market.	**K2**
CO4	Make use of the possibilities of value analysis and engineering, and solve simple business problems using break even analysis, cost benefit analysis and capital budgeting techniques.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	-	-	-	-	-	1	-	-	-	-	1	-
CO2	-	-	-	-	-	1	1	-	-	-	1	-
CO3	-	-	-	-	1	-	-	-	-	-	2	-
CO4	-	-	-	-	1	1	-	-	-	-	2	-

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Managerial Economics	Geetika, Piyali Ghosh and Chodhury	Tata McGraw Hill,	2015
2	Engineering Economy	H. G. Thuesen, W. J. Fabrycky	PHI	1966
3	Engineering Economics	R. Paneerselvam	PHI	2012

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Engineering Economy	Leland Blank P.E, Anthony Tarquin P. E.	Mc Graw Hill	7TH Edition
2	Indian Financial System	Khan M. Y.	Tata McGraw Hill	2011
3	Engineering Economics and analysis	Donald G. Newman, Jerome P. Lavelle	Engg. Press, Texas	2002
4	Contemporary Engineering Economics	Chan S. Park	Prentice Hall of India Ltd	2001

SEMESTER S3/S4

ENGINEERING ETHICS AND SUSTAINABLE DEVELOPMENT

Course Code	**UCHUT347**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	2:0:0:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Equip with the knowledge and skills to make ethical decisions and implement gender-sensitive practices in their professional lives.
2. Develop a holistic and comprehensive interdisciplinary approach to understanding engineering ethics principles from a perspective of environment protection and sustainable development.
3. Develop the ability to find strategies for implementing sustainable engineering solutions.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Fundamentals of ethics** - Personal vs. professional ethics, Civic Virtue, Respect for others, **Profession and Professionalism,** Ingenuity, diligence and responsibility, Integrity in design, development, and research domains, Plagiarism, a balanced outlook on law - challenges - case studies, **Technology and digital revolution**-Data, information, and knowledge, Cybertrust and cybersecurity, Data collection & management, **High technologies: connecting people and places**-accessibility and social impacts, **Managing conflict**, Collective bargaining, **Confidentiality**, Role of confidentiality in moral integrity, **Codes of Ethics**. **Basic concepts in Gender Studies** - sex, gender, sexuality, gender spectrum: beyond the binary, gender identity, gender expression, gender stereotypes, **Gender disparity and discrimination in education**,	**6**

	employment and everyday life, History of women in Science & Technology, Gendered technologies & innovations**, Ethical values and practices in connection with gender** - equity, diversity & gender justice, **Gender policy and women/transgender empowerment initiatives.**	
2	**Introduction to Environmental Ethics:** Definition, importance and historical development of environmental ethics, key philosophical theories (anthropocentrism, biocentrism, ecocentrism). **Sustainable Engineering Principles:** Definition and scope, triple bottom line (economic, social and environmental sustainability), life cycle analysis and sustainability metrics. **Ecosystems and Biodiversity:** Basics of ecosystems and their functions, Importance of biodiversity and its conservation, Human impact on ecosystems and biodiversity loss, An overview of various ecosystems in Kerala/India, and its significance. **Landscape and Urban Ecology:** Principles of landscape ecology, Urbanization and its environmental impact, Sustainable urban planning and green infrastructure.	**6**
3	**Hydrology and Water Management:** Basics of hydrology and water cycle, Water scarcity and pollution issues, Sustainable water management practices, Environmental flow, disruptions and disasters. **Zero Waste Concepts and Practices:** Definition of zero waste and its principles, Strategies for waste reduction, reuse, reduce and recycling, Case studies of successful zero waste initiatives. **Circular Economy and Degrowth:** Introduction to the circular economy model, Differences between linear and circular economies, degrowth principles, Strategies for implementing circular economy practices and degrowth principles in engineering. **Mobility and Sustainable Transportation:** Impacts of transportation on the environment and climate, Basic tenets of a Sustainable Transportation design, Sustainable urban mobility solutions, Integrated mobility systems, E-Mobility, Existing and upcoming models of sustainable mobility solutions.	**6**
4	**Renewable Energy and Sustainable Technologies:** Overview of renewable energy sources (solar, wind, hydro, biomass), Sustainable technologies in energy production and consumption, Challenges and opportunities in renewable energy adoption. **Climate Change and Engineering Solutions:** Basics of climate change science, Impact of climate change on natural and human systems, Kerala/India and the Climate crisis, Engineering solutions to mitigate, adapt and build resilience to climate change. **Environmental**	**6**

	Policies and Regulations: Overview of key environmental policies and regulations (national and international), Role of engineers in policy implementation and compliance, Ethical considerations in environmental policy-making. **Case Studies and Future Directions:** Analysis of real-world case studies, Emerging trends and future directions in environmental ethics and sustainability, Discussion on the role of engineers in promoting a sustainable future.	

Course Assessment Method
(CIE: 50 marks , ESE: 50)

Continuous Internal Evaluation Marks (CIE):

Continuous internal evaluation will be based on individual and group activities undertaken throughout the course and the portfolio created documenting their work and learning. The portfolio will include reflections, project reports, case studies, and all other relevant materials.

- The students should be grouped into groups of size 4 to 6 at the beginning of the semester. These groups can be the same ones they have formed in the previous semester.
- Activities are to be distributed between 2 class hours and 3 Self-study hours.
- The portfolio and reflective journal should be carried forward and displayed during the 7th Semester Seminar course as a part of the experience sharing regarding the skills developed through various courses.

Sl. No.	Item	Particulars	Group/ Individual (G/I)	Marks
1	Reflective Journal	Weekly entries reflecting on what was learned, personal insights, and how it can be applied to local contexts.	I	5
2	Micro project (Detailed documentation of the project, including methodologies, findings, and reflections)	1 a) Perform an Engineering Ethics Case Study analysis and prepare a report 1 b) Conduct a literature survey on 'Code of Ethics for Engineers' and prepare a sample code of ethics	G	8
		2. Listen to a TED talk on a Gender-related topic, do a literature survey on that topic and make a report citing the relevant papers with a specific analysis of the Kerala context	G	5
		3. Undertake a project study based on the concepts of sustainable development* - Module II, Module III & Module IV	G	12
3	Activities	2. One activity* each from Module II, Module III & Module IV	G	15
4	Final Presentation	A comprehensive presentation summarising the key takeaways from the course, personal reflections, and proposed future actions based on the learnings.	G	5
		Total Marks		**50**

*Can be taken from the given sample activities/projects

Evaluation Criteria:

- **Depth of Analysis**: Quality and depth of reflections and analysis in project reports and case studies.
- **Application of Concepts**: Ability to apply course concepts to real-world problems and local contexts.
- **Creativity**: Innovative approaches and creative solutions proposed in projects and reflections.
- **Presentation Skills**: Clarity, coherence, and professionalism in the final presentation.

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Develop the ability to apply the principles of engineering ethics in their professional life.	**K3**
CO2	Develop the ability to exercise gender-sensitive practices in their professional lives	**K4**
CO3	Develop the ability to explore contemporary environmental issues and sustainable practices.	**K5**
CO4	Develop the ability to analyse the role of engineers in promoting sustainability and climate resilience.	**K4**
CO5	Develop interest and skills in addressing pertinent environmental and climate-related challenges through a sustainable engineering approach.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1						3	2	3	3	2		2
CO2		1				3	2	3	3	2		2
CO3						3	3	2	3	2		2
CO4		1				3	3	2	3	2		2
CO5						3	3	2	3	2		2

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Ethics in Engineering Practice and Research	Caroline Whitbeck	Cambridge University Press & Assessment	2nd edition & August 2011
2	Virtue Ethics and Professional Roles	Justin Oakley	Cambridge University Press & Assessment	November 2006
3	Sustainability Science	Bert J. M. de Vries	Cambridge University Press & Assessment	2nd edition & December 2023
4	Sustainable Engineering Principles and Practice	Bhavik R. Bakshi,	Cambridge University Press & Assessmen	2019
5	Engineering Ethics	M Govindarajan, S Natarajan and V S Senthil Kumar	PHI Learning Private Ltd, New Delhi	2012
6	Professional ethics and human values	RS Naagarazan	New age international (P) limited New Delhi	2006.
7	Ethics in Engineering	Mike W Martin and Roland Schinzinger,	Tata McGraw Hill Publishing Company Pvt Ltd, New Delhi	4" edition, 2014

Suggested Activities/Projects:

Module-II

- Write a reflection on a local environmental issue (e.g., plastic waste in Kerala backwaters or oceans) from different ethical perspectives (anthropocentric, biocentric, ecocentric).
- Write a life cycle analysis report of a common product used in Kerala (e.g., a coconut, bamboo or rubber-based product) and present findings on its sustainability.
- Create a sustainability report for a local business, assessing its environmental, social, and economic impacts
- Presentation on biodiversity in a nearby area (e.g., a local park, a wetland, mangroves, college campus etc) and propose conservation strategies to protect it.
- Develop a conservation plan for an endangered species found in Kerala.
- Analyze the green spaces in a local urban area and propose a plan to enhance urban ecology using native plants and sustainable design.

- Create a model of a sustainable urban landscape for a chosen locality in Kerala.

Module-III

- Study a local water body (e.g., a river or lake) for signs of pollution or natural flow disruption and suggest sustainable management and restoration practices.
- Analyse the effectiveness of water management in the college campus and propose improvements - calculate the water footprint, how to reduce the footprint, how to increase supply through rainwater harvesting, and how to decrease the supply-demand ratio
- Implement a zero waste initiative on the college campus for one week and document the challenges and outcomes.
- Develop a waste audit report for the campus. Suggest a plan for a zero-waste approach.
- Create a circular economy model for a common product used in Kerala (e.g., coconut oil, cloth etc).
- Design a product or service based on circular economy and degrowth principles and present a business plan.
- Develop a plan to improve pedestrian and cycling infrastructure in a chosen locality in Kerala

Module-IV

- Evaluate the potential for installing solar panels on the college campus including cost-benefit analysis and feasibility study.
- Analyse the energy consumption patterns of the college campus and propose sustainable alternatives to reduce consumption - What gadgets are being used? How can we reduce demand using energy-saving gadgets?
- Analyse a local infrastructure project for its climate resilience and suggest improvements.
- Analyse a specific environmental regulation in India (e.g., Coastal Regulation Zone) and its impact on local communities and ecosystems.
- Research and present a case study of a successful sustainable engineering project in Kerala/India (e.g., sustainable building design, water management project, infrastructure project).
- Research and present a case study of an unsustainable engineering project in Kerala/India highlighting design and implementation faults and possible corrections/alternatives (e.g., a housing complex with water logging, a water management project causing frequent floods, infrastructure project that affects surrounding landscapes or ecosystems).

SEMESTER S3

ANALOG CIRCUITS LAB

Course Code	**PCECL307**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Lab

Course Objectives:

1. Familiarise the students with the analog circuits design using discrete components.
2. Familiarise the students with simulation of basic analog circuits.

Expt. No.	Part A – List of Experiments using discrete components (Any *Six* experiments mandatory)
1	RC Integrating and Differentiating Circuits – (Transient analysis with different inputs and frequency response)
2	Diode Clipping and Clamping Circuits (Transient and transfer characteristics)
3	CE amplifier – Design for a specific voltage gain and plot frequency response characteristics
4	CS MOSFET amplifier - Design for a specific voltage gain and plot frequency response characteristics
5	Cascaded amplifier (CE – CE) - Design for a specific voltage gain and plot frequency response characteristics
6	Cascode amplifier - Design for a specific voltage gain and plot frequency response characteristics
7	Feedback amplifiers (current series & voltage series) - Design for a specific voltage gain and plot frequency response characteristics
8	RC oscillators – RC phase shift or wien bridge oscillator
9	Power amplifiers (Transformer less) – Class B & Class AB
10	Transistor series voltage regulator – Design for a specific output voltage with & without short circuit protection (plot load & line regulation characteristics).
Expt. No.	**Part B – Simulation Experiments (Any *Six* experiments mandatory)** The experiments shall be conducted using Open-Source Tools such as QUCS, KiCad, LT SPICE, or variants of SPICE tools.
1	RC Integrating and Differentiating Circuits – (Transient analysis with different inputs and frequency response)
2	Diode Clipping and Clamping Circuits (Transient and transfer characteristics)
3	CE amplifier – Design for a specific voltage gain and plot frequency response characteristics

4	CS MOSFET amplifier - Design for a specific voltage gain and plot frequency response characteristics
5	Cascaded amplifier (CE – CE) - Design for a specific voltage gain and plot frequency response characteristics
6	Cascode amplifier - Design for a specific voltage gain and plot frequency response characteristics
7	Feedback amplifiers (current series & voltage series) - Design for a specific voltage gain and plot frequency response characteristics
8	RC oscillators – RC phase shift or wien bridge oscillator
9	Power amplifiers (Transformer less) – Class B & Class AB
10	Transistor series voltage regulator – Design for a specific output voltage with & without short circuit protection (plot load & line regulation characteristics).

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	**15**	**10**	**10**	**5**	**50**

- ***Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.***
- ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design and demonstrate the functioning of basic analog circuits using discrete components.	**K3**
CO2	Design and simulate the functioning of basic analog circuits using simulation tools.	**K3**
CO3	Conduct troubleshooting of a given circuit and to analyze it	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2						3			3
CO2	3	2	2		3				3			3
CO3	3	2	2						3			3

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Electronic Devices and Circuits	David A Bell	Oxford University Press, 2008	5th edition
2	Electronic Circuits Analysis and Design 1	D. Meganathan	Yes Dee Publishing, 2023	1st edition

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. **Conduct of Experiments (7 Marks)**

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. **Lab Reports and Record Keeping (6 Marks)**

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
- Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. **Result with Valid Inference/Quality of Output (10 Marks)**

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. Viva Voce (10 Marks)

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. Record (5 Marks)

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER S3

LOGIC CIRCUIT DESIGN LABORATORY

Course Code	**PCECL308**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Lab

Course Objectives:

1. Familiarise the students with the Digital Logic Design through the implementation of Logic Circuits .
2. Familiarise the students with the HDL based Digital Design and FPGA boards.

Expt. No.	**Part A – List of Experiments using digital components (Any *Six* experiments mandatory)**
1	Realization of functions using basic and universal gates (SOP and POS forms).
2	Design and Realization of half/full adder and subtractor using basic gates and universal gates.
3	4 bit adder/subtractor and BCD adder using 7483
4	Study of Flip Flops : S-R, D, T, JK and Master slave JK FF using NAND gates
5	Asynchronous Counter : 3 bit up/down counter, Realization of Mod N Counter
6	Synchronous Counter: Realization of 4-bit up/down counter, Realization of Mod-N counters
7	Ring counter and Johnson Counter.
8	Realization of counters using IC's (7490, 7492, 7493).
9	Realization of combinational circuits using MUX & DEMUX, using ICs (74150, 74154)
10	Sequence Generator / Detector
Expt. No.	**Part B – Simulation Experiments (Any *Six* experiments mandatory)** The experiments shall be conducted using Verilog and implementation using small FPGA
1	Realization of Logic Gates and Familiarization of FPGAs (a) Familiarization of a small FPGA board and its ports and interface. (b) Create the .pcf files for your FPGA board. (c) Familiarization of the basic syntax of verilog

	(d) Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables. (e) Verify the universality and non associativity of NAND and NOR gates by uploading The corresponding verilog files to the FPGA boards.
2	Adders in Verilog (a) Development of verilog modules for half adder in any of the 3 modeling styles (b) Development of verilog modules for full adder in structural modeling using half adder.
3	Mux and Demux in Verilog (a) Development of verilog modules for a 4x1 MUX. (b) Development of verilog modules for a 1x4 DEMUX.
4	Flipflops and coutners (a) Development of verilog modules for SR, JK and D flipflops. (b) Development of verilog modules for a binary decade/Johnson/Ring counters
5	Multiplexer and Logic Implementation in FPGA (a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality. (b) Use the above module to realize any logic function
6	Flip-Flops and their Conversion in FPGA (a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board. (b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D
7	Asynchronous and Synchronous Counters in FPGA (a) Make a design of a 4-bit up down ripple counter using T-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGAboard.
8	Universal Shift Register in FPGA (a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Implement ring and Johnson counters with it.
9	BCD to Seven Segment Decoder in FPGA (a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality. (b) Test it with switches and seven segment display. Use ouput ports for connection to the display.

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

- ***Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.***
- ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design and demonstrate the functioning of various combinational and sequential circuits using ICs	**K3**
CO2	Apply an industry compatible hardware description language to implement digital circuits	**K3**
CO3	Implement digital circuits on FPGA boards and connect external hardware to the boards	**K3**
CO4	Function effectively as an individual and in a team to accomplish the given task.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2					3			3
CO2	3	1	1	3	3				3	1		3
CO3	3	1	1	3	3				3	1		3
CO4	3	3	3		3				3			3

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL Synthesis: A Practical Primer	. J. Bhasker	B. S. Publications, 2001	
2	Fundamentals of Logic Design	Roth C.H	Jaico Publishers. V Ed., 2009	5th Edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL :A guide to digital design and synthesis	Palnitkar S.,	Prentice Hall; 2003.	2nd Edn.,

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. Lab Reports and Record Keeping (6 Marks)

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
- Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. **Result with Valid Inference/Quality of Output (10 Marks)**

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. **Viva Voce (10 Marks)**

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. **Record (5 Marks)**

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER 4

ELECTRONICS ENGINEERING (VLSI Design and Technology)

SEMESTER S4

MATHEMATICS FOR ELECTRICAL SCIENCE - 4

Course Code	GAMAT401	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Basic calculus	Course Type	Theory

Course Objectives:

1. To familiarize students with the foundations of probabilistic and statistical analysis mostly used in varied applications in engineering and science.
2. To familiarize students with the basics of random processes essential for their subsequent study of analog and digital communication.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Random variables, Discrete random variables and their probability distributions, Cumulative distribution function, Expectation, Mean and variance, Binomial distribution, Poisson distribution, Poisson distribution as a limit of the binomial distribution, Joint pmf of two discrete random variables, Marginal pmf, Independent random variables, Expected value of a function of two discrete variables. **[Text 1: Relevant topics from sections 3.1 to 3.4, 3.6, 5.1, 5.2]**	9
2	Continuous random variables and their probability distributions, Cumulative distribution function, Expectation, Mean and variance, Uniform, Normal and Exponential distributions, Joint pdf of two Continuous random variables, Marginal pdf, Independent random variables, Expectation value of a function of two continuous variables. **[Text 1: Relevant topics from sections 3.1, 4.1, 4.2, 4.3, 4.4, 5.1, 5.2]**	9

3	Confidence Intervals, Confidence Level, Confidence Intervals and One-side confidence intervals for a Population Mean for large and small samples (normal distribution and t-distribution), Hypotheses and Test Procedures, Type I and Type II error, z Tests for Hypotheses about a Population Mean (for large sample), t Test for Hypotheses about a Population Mean (for small sample), Tests concerning a population proportion for large and small samples. **[Text 1: Relevant topics from 7.1, 7.2, 7.3, 8.1, 8.2, 8.3, 8.4]**	**9**
4	Random process concept, classification of process, Methods of Description of Random process, Special classes, Average Values of Random Process, Stationarity- SSS, WSS, Autocorrelation functions and its properties, Ergodicity, Mean-Ergodic Process, Mean-Ergodic Theorem, Correlation Ergodic Process, Distribution Ergodic Process. **[Text 2: Relevant topics from Chapter 6]**	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the concept, properties and important models of discrete random variables and to apply in suitable random phenomena.	**K3**
CO2	Understand the concept, properties and important models of continuous random variables and to apply in suitable random phenomena.	**K3**
CO3	Estimate population parameters, assess their certainty with confidence intervals, and test hypotheses about population means and proportions using z-tests and the one-sample t-test.	**K3**
CO4	Analyze random processes by classifying them, describing their properties , utilizing autocorrelation functions, and understanding their applications in areas like signal processing and communication systems..	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**-**	**2**	-	-	-	-	-	-	-	**2**
CO2	**3**	**3**	**-**	**2**	-	-	-	-	-	-	-	**2**
CO3	**3**	**3**	**-**	**2**	-	-	-	-	-	-	-	**2**
CO4	**3**	**3**	**-**	**2**	-	-	-	-	-	-	-	**2**

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Probability and Statistics for Engineering and the Sciences	Devore J. L	Cengage Learning	9th edition, 2016
2	Probability, Statistics and Random Processes	T Veerarajan	The McGraw-Hill	3rd edition,2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Probability, Random Variables and Stochastic Processes,	Papoulis, A. & Pillai, S.U.,	McGraw Hill.	4th edition, 2002
2	Introduction to Probability and Statistics for Engineers and Scientists	Ross, S. M.	Elsevier	4th edition, 2004
3	Probability and Random Processes	Palaniammal, S.	PHI Learning Private Limited	3rd edition, 2015
4	Introduction to Probability	David F. Anderson, Timo, Benedek	Cambridge	2017

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/105/117105085/
2	https://archive.nptel.ac.in/courses/117/105/117105085/
4	https://archive.nptel.ac.in/courses/117/105/117105085/

SEMESTER S4

DIGITAL SYSTEM DESIGN

Course Code	PCEVT402	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304 Logic Circuit Design	Course Type	Theory

Course Objectives:

1. To equip students with comprehensive knowledge and skills in designing, analysing, modelling, and optimizing clocked synchronous sequential networks (CSSNs).
2. To provide a thorough understanding of the designing, analyzing, and optimizing techniques of asynchronous sequential circuits (ASCs).
3. To equip students with the knowledge and skills to identify and mitigate static and dynamic hazards and to understand fault detection and testing methods.
4. To provide students with a comprehensive understanding of the VLSI design flow and the application of VHDL constructs and coding for combinational and sequential circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Clocked Synchronous Networks, Analysis of Clocked Synchronous Sequential Networks (CSSN), Modelling of CSSN, State assignment and reduction, Design of CSSN, ASM Chart and its realization.	11
2	Asynchronous Sequential Circuits, Analysis of Asynchronous Sequential Circuits (ASC), Flow table reduction, Races in ASC, State assignment problem and the transition table, Design of Asynchronous Sequential Circuits, Design of ALU.	11
3	Hazards – static and dynamic hazards in combinational networks, Essential Hazards, Design of Hazard free circuits, Data synchronizers, Mixed operating mode asynchronous circuits, Practical issues- clock skew and jitter, Synchronous and asynchronous inputs, Flip-Flops and	11

	Simple Flip-Flop Applications, switch debouncer. Faults, Fault table method – path sensitization method – Boolean difference method, Kohavi algorithm, Automatic test pattern generation – Built in Self-Test (BIST)	
4	VLSI Design flow: Design entry: Schematic, FSM & HDL, different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling, Synthesis, simulation. VHDL constructs and codes for combinational and sequential circuits.	**11**

Course Assessment Method
(CIE: 40 mark , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design, analyze, and model clocked synchronous sequential networks (CSSNs), optimize state assignment and reduction, and effectively utilize ASM charts for the realization of complex digital systems.	**K3**
CO2	Design and analyze asynchronous sequential circuits (ASCs), perform flow table reduction, address race conditions and state assignment problems, and design both ASCs and Arithmetic Logic Units (ALUs).	**K3**
CO3	Identify and mitigate static and dynamic hazards in combinational networks, design hazard-free circuits, address practical issues in digital systems and apply fault detection and testing methods.	**K2**
CO4	Understand the VLSI design flow, utilize various design entry methods, apply different VHDL modeling styles, and develop and simulate VHDL constructs for combinational and sequential circuits.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**	**2**									
CO2	**3**	**2**	**2**									
CO3	**3**	**1**	**2**									
CO4	**1**	**1**	**2**	**1**	**2**							
CO5												

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Principles & Design	Donald G Givone	McGraw Hill Education	2017
2	Digital Design: Principles and Practices	John F Wakerly	Pearson India	4th, 2008
3	Digital Logic Applications and Design	John M Yarbrough	Cengage Learning India	1st, 2006
4	Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog	M.Morris Mano and Michel.D.Ciletti,	Pearson	6th, 2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Systems Testing and Testable Design	Melvin A. Breuer, Miron Abramovici, Arthur D. Friedman	Wiley-IEEE Press	1st, 1994
2	Logic Design Theory	Nripendra N. Biswas	Prentice Hall	1993
3	Introduction to Digital Design Using Digilent FPGA Boards: Block Diagram / VHDL Examples	Richard E. Haskell Darrin M. Hanna	LBE Books- LLC	2019
4	Digital Circuits and Logic Design	Samuel C. Lee	Prentice Hall India Learning Private Limited	1980
5	Switching and Finite Automata Theory	Zvi Kohavi, Niraj K. Jha	CAMBRIDGE UNIVERSITY PRESS	3rd 2009
6	Digital System Design Using VHDL	Rishabh Anand	Khanna Publishing	1st, 2013
7	Digital System Design Using VHDL	Lizy Kurian John, Charles H. Roth	Cengage	1st, 2012

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/
2	https://archive.nptel.ac.in/courses/117/106/117106086/
3	https://archive.nptel.ac.in/courses/108/105/108105132/ Lecture 15
4	https://nptel.ac.in/courses/108106177

SEMESTER S4

LINEAR INTEGRATED CIRCUITS

Course Code	PCECT403	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Analog Circuits (PCECT303)	Course Type	Theory

Course Objectives:

1. To develop skills to design and analyze circuits using operational amplifiers for various applications.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Differential Amplifiers:** Differential amplifier configurations using BJT, DC Analysis - transfer characteristics; AC analysis - differential and common mode gains, CMRR, input and output resistance, voltage gain, constant current bias, constant current source. **Concept of current mirror**: two-transistor current mirror, Wilson and Widlar current mirrors. **Operational amplifiers (Op Amps):** The 741 Op Amp, Block diagram, Ideal Op Amp parameters, typical parameter values for 741, equivalent circuit, open loop configurations, voltage transfer curve, frequency response curve.	11
2	**Op Amp with negative feedback:** General concept of Voltage Series, Voltage Shunt, Current Series and Current Shunt negative feedback, Op Amp circuits with Voltage Series and Voltage Shunt feedback, Virtual ground concept. Analysis of inverting and non-inverting amplifier for closed loop gain, Input Resistance and Output Resistance. **Op Amp applications:** Summer, Voltage Follower, Differential and Instrumentation Amplifiers, Voltage to Current and Current to Voltage converters, Integrator, Differentiator, Precision Rectifiers, Comparators,	11

	Schmitt Triggers, Log and Antilog amplifiers.	
3	**Oscillators and Multivibrators:** Phase Shift and Wien-bridge Oscillators, Triangular and Sawtooth waveform generators, Astable and Monostable multivibrators. **Active filters:** Comparison with passive filters, First and Second order Low pass, High pass, Band pass and Band Reject active filters, State Variable filters. **Voltage Regulators:** Fixed and Adjustable voltage regulators, IC 723 – Low voltage and High voltage configurations, Current boosting, Current limiting, Short circuit and Fold-back protection.	**11**
4	**Timer and VCO:** Timer IC 555 - Functional diagram, Astable and monostable operations, Basic concepts of Voltage Controlled Oscillator and application of VCO IC LM566. **Phase Locked Loop**: Basic building block, Operation, Closed loop analysis, Lock and capture range, Applications of PLL, PLL IC565. **Data Converters:** Digital to Analog converters, Specifications, Weighted resistor type and R-2R Ladder type. Analog to Digital Converters: Specifications, Flash type and Successive approximation type.	**11**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Summarize the concepts of operational amplifiers and differential amplifier configurations	**K2**
CO2	Design operational amplifier circuits for various applications.	**K3**
CO3	Choose integrated circuit chips for various linear circuit applications.	**K2**
CO4	Implement various applications using specific integrated circuit chips	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2										1
CO2	3	2	3	3	2							2
CO3	3				2							2
CO4	3	2	2	2	2							2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Linear Integrated Circuits	Roy D. C. and S. B. Jain	New Age International	5/e, 2018

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design with Operational Amplifiers and Analog Integrated Circuits	Sergio Franco	Tata McGraw Hill	3/e, 2017
2	Op-Amps and Linear Integrated Circuits	Gayakwad R. A.	Prentice Hall	4/e, 2015
3	Integrated Circuits	Botkar K. R.	Khanna Publishers	10/e, 2013
4	Operational Amplifiers	C.G. Clayton	Butterworth & Company Publ. Ltd. Elsevier	5/e, 2005
5	Operational Amplifiers & Linear Integrated Circuits	R.F. Coughlin & Fredrick Driscoll	PHI	6/e, 2000
6	Operational Amplifiers & Linear ICs	David A. Bell	Oxford University Press	3/e, 2011
7	Microelectronic Circuits	Sedra A. S. and K. C. Smith	Oxford University Press	6/e, 2013

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117101106
2	https://nptel.ac.in/courses/117101106
3	https://nptel.ac.in/courses/117101106
4	https://nptel.ac.in/courses/117101106

SEMESTER S4

MICROCONTROLLERS & EMBEDDED SYSTEMS

Course Code	PBECT404	CIE Marks	60
Teaching Hours/Week (L: T:P: R)	3:0:0:1	ESE Marks	40
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304-Logic Circuit Design	Course Type	Theory

Course Objectives:

1. To learn Microcontroller architecture and its programming
2. To learn Embedded system design to develop a product.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Microcontroller Architecture – General internal architecture, Address bus, Data bus, control bus. The Microcontroller 8051: Features of 8051 microcontroller, Block diagram of 8051- program status word (PSW), accumulator, program counter. Memory organization – RAM & ROM, register banks and stack, Special Function Registers (SFRs), I/O port organization, Interrupts.	9
2	Instruction Set of 8051 & Addressing modes: Classification of instruction set - Data transfer group, arithmetic group, logical group, branching group. Addressing modes - Types. Accessing the data from internal and external memory.	9
3	Programming 8051 Using Assembly Language: Introduction to 8051 assembly language programming. Data types & directives, Concept of subroutine. Software delay programming. Programming 8051 Using Embedded C Language: Introduction to embedded C – advantages.	9
4	Timer / Counter in 8051: Timer registers - Timer0, Timer1. Configuration of timer registers. Timer mode programming. Counter	9

	mode. Serial Communication in 8051: Serial communication – modes and protocols, RS-232 pin configuration and connection. Serial port programming – transmitting and receiving. Programming the interrupts: Use external, timer and serial port interrupts. Interrupt priority settings.	

Suggestion on Project Topics

1. Interface any known ADC chip to 8051 uC. Read the variation in voltage from a potentiometer and display it on an LCD module.
2. Interface any known DAC chip to 8051 uC. Generate a Sine waveform of 1KHz at any port pin.
3. DC motor interface for speed and direction control.
4. Stepper motor interface - Unit step control, Rotation angle control, Speed control, Direction control
5. Read the Temperature sensor and display it on LCD.

Course Assessment Method
(CIE: 60 marks, ESE: 40 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Project	Internal Ex-1	Internal Ex-2	Total
5	30	12.5	12.5	60

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 2 marks **(8x2 =16 marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 2 sub divisions. • Each question carries 6 marks. **(4x6 = 24 marks)**	**40**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Outline Architecture of Microcontroller	**K2**
CO2	Develop Microcontroller programs	**K5**
CO3	Design various interfaces to Microcontroller	**K5**
CO4	Design and implement an Embedded System	**K6**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3											
CO2	3	3	3	2	3			2				2
CO3	3	3	3	3	3			2				2
CO4	3	3	3	3	3	3	3	3	3	3	3	3

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	The 8051 Microcontroller and Embedded Systems Using Assembly and C	Muhammad Ali Mazidi Janice Gillispie Mazidi Rolin D. McKinlay	Prentice Hall -Inc	Second, 2007
2	The 8051 Microcontroller Architecture, Programming and Applications	Kenneth J Ayala Dhananjay V Gadre	Cengage Learning	2010

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	8051 hardware Description	Datasheet	Intel Corporation	1992
2	Microprocessors and Microcontrollers	Lyla B. Das	Pearson Education	2011

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	Microprocessors and Microcontrollers - https://nptel.ac.in/courses/106108100
2	Microcontrollers and Applications - https://nptel.ac.in/courses/117104072

PBL Course Elements

L: Lecture (3 Hrs.)	**R: Project (1 Hr.), 2 Faculty Members**		
	Tutorial	**Practical**	**Presentation**
Lecture delivery	Project identification	Simulation/ Laboratory Work/ Workshops	Presentation (Progress and Final Presentations)
Group discussion	Project Analysis	Data Collection	Evaluation
Question answer Sessions/ Brainstorming Sessions	Analytical thinking and self-learning	Testing	Project Milestone Reviews, Feedback, Project reformation (If required)
Guest Speakers (Industry Experts)	Case Study/ Field Survey Report	Prototyping	Poster Presentation/ Video Presentation: Students present their results in a 2 to 5 minutes video

Assessment and Evaluation for Project Activity

Sl. No	**Evaluation for**	**Allotted Marks**
1	Project Planning and Proposal	5
2	Contribution in Progress Presentations and Question Answer Sessions	4
3	Involvement in the project work and Team Work	3
4	Execution and Implementation	10
5	Final Presentations	5
6	Project Quality, Innovation and Creativity	3
Total		**30**

1. **Project Planning and Proposal (5 Marks)**

- Clarity and feasibility of the project plan
- Research and background understanding
- Defined objectives and methodology

2. Contribution in Progress Presentation and Question Answer Sessions (4 Marks)

- Individual contribution to the presentation
- Effectiveness in answering questions and handling feedback

3. **Involvement in the Project Work and Team Work (3 Marks)**

- Active participation and individual contribution
- Teamwork and collaboration

4. **Execution and Implementation (10 Marks)**

- Adherence to the project timeline and milestones
- Application of theoretical knowledge and problem-solving
- Final Result

5. **Final Presentation (5 Marks)**

- Quality and clarity of the overall presentation
- Individual contribution to the presentation
- Effectiveness in answering questions

6. **Project Quality, Innovation, and Creativity (3 Marks)**

- Overall quality and technical excellence of the project
- Innovation and originality in the project
- Creativity in solutions and approaches

SEMESTER S4

ELECTROMAGNETIC WAVES

Course Code	PEEVT411	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Probability, Random Process and Numerical Methods GBMAT401	Course Type	Theory

Course Objectives:

1. To analyse different analog and digital communication systems.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Block diagram of a communication system. Need for modulation. Amplitude modulation, Equation and spectrum of AM signal, DSB-SC, SSB -pilot carrier and Vestigial sideband systems. Angle modulation: Narrow and wide band FM and their spectra, relationship between FM and PM, Carson's rule, pre-emphasis and de-emphasis filtering. Comparison of AM and FM. Superheterodyne receivers- Characteristics of receivers –image frequency. Noise: external, internal, White noise.	12
2	Sampling and Quantization, SQNR for uniform quantization, Companding Pulse code modulation, Transmitter and receiver. DPCM transmitter and receiver.Delta modulation, Slope overload, Line codes.	10
3	Baseband data transmission of digital data through AWGN channel, Mathematical model of ISI, Nyquist criterion for zero ISI, Signal modelling for ISI, Raised cosine spectrum, Equalization. Geometric representation of Signals-Gram-Schmitt procedure, Signal space. Vector model of AWGN channel. Matched filter and correlation receivers, MAP receiver, Maximum likelihood receiver.	12

4	Digital band pass modulation schemes-BPSK system and signal constellation. BPSK transmitter and receiver. QPSK system and Signal constellations. Plots of BER Vs SNR with analysis. QPSK transmitter and receiver. Quadrature amplitude modulation and signalconstellation.	**10**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Illustrate the principles of analog communication systems	**K2**
CO2	Explain the basic concepts of digital communication	**K2**
CO3	Analyse the baseband transmission of digital data through AWGN channel	**K3**
CO4	Apply various digital modulation techniques in the design of digital communication systems	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	2	-	-	-	-	-	-	-
CO2	3	-	-	-	2	-	-	-	-	-	-	-
CO3	3	3	3	3	2	-	-	-	-	-	-	2
CO4	3	3	3	3	2	-	-	-	-	-	-	2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Communication Systems	Simon Haykin and Michael Moher	Wiley	5th Edition, 2020
2	Modern Digital and Analog Communication Systems	B.P. Lathi and Zhi Ding	Oxford University Press	5th Edition, 2018
3	Introduction to Analog and Digital Communication	Simon Haykin and Michael Moher	Wiley	2nd Edition, 2006

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Principles of Communication Systems	Herbert Taub and Donald L. Schilling	McGraw-Hill Education	4th Edition, 2013
2	Digital Communications	John G. Proakis and Masoud Salehi	McGraw-Hill Education	6th Edition, 2020
3	Communication Systems Engineering	John G. Proakis and Masoud Salehi	Pearson	2nd Edition, 2001
4	Digital Communications	Simon Haykin	John Wiley& Sons	4th Edition, 2015
5	Electronic communication systems	George Kennedy McGraw Hill 6th Edition, 2017	George Kennedy McGraw Hill 6th Edition, 2017	George Kennedy McGraw Hill 6th Edition, 2017

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/hTAlcrqjNps?si=okoRHdUegx9pbOz3
2	https://youtu.be/s_vmLqT_6NQ?si=MF2OW6AaICiYKTfj

SEMESTER S4

LINUX AND SCRIPTING

Course Code	**PEEVT412**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	-	**Course Type**	Theory

Course Objectives:

1. This course aims to provide students with a comprehensive understanding of Linux operating systems and scripting languages, specifically Python and TCL, in the context of Very Large Scale Integration (VLSI) design
2. Students will learn how to leverage the power of Linux for VLSI applications, automate design processes using Python and TCL scripts

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Linux Kernel:** System Memory Management, Software Program Management, Hardware Management, Filesystem Management. **Linux Desktop Environment:** The X Window System, KDE Desktop, GNOME Desktop, Unity Desktop. **Linux Distributions:** Core Linux Distributions, Specialized Linux Distributions	**9**
2	**Shell :**Reaching the Command Line, Console Terminals , Graphical Terminals, Accessing CLI via a Linux Console Terminal, Accessing CLI via Graphical Terminal Emulation, Using the GNOME Terminal Emulator, Accessing the GNOME Terminal, Using the xterm Terminal Emulator, Accessing xterm.	**9**

3	**Basic Shell Commands:** Starting the Shell, Using the Shell Prompt, Interacting with the bash Manual, Looking at the Linux file system, Traversing directories, Listing Files and Directories, Handling Files, Copying files, Deleting files, Creating directories, Deleting directories. **Linux Security:** Removing a user, Modifying a user, Using file permission symbols, Default file permissions, Changing permissions, Changing ownership, Sharing Files.	**9**
4	**Vim Editor:** Introduction to vim Features, Command Mode: Moving the Cursor, Input Mode, Command Mode: Deleting and Changing Text, Reading and Writing Files. **Python scripting:** Data structures, modules, inputs and outputs, Floating Point Arithmetic: Issues and Limitations.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the Linux operating system and demonstrate proficiency in command-line usage for VLSI design	**K2**
CO2	Develop TCL scripts for automating tasks and extending functionality in VLSI design environments	**K3**
CO3	Demonstrate proficiency in handling files, including copying, deleting, creating, and deleting directories using basic shell commands	**K3**
CO4	Develop Python scripts for automation, data analysis, and interaction with VLSI design tools	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**1**	**2**		**2**							**1**
CO2	**3**	**1**	**2**		**2**							**1**
CO3	**3**	**1**	**2**		**2**							**1**
CO4	**3**	**1**	**2**		**2**							**1**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	A Practical Guide to Linux® Commands, Editors, and Shell Programming	Guido van Rossum	Prentice Hall PTR	1/e, 2005
2	An Introduction to Python	Giuseppe Massobrio	Network Theory Limited	1/e, 2001
3	Linux® Command Line and Shell Scripting Bible	Richard Blum	Wiley	3/e, 2015
4	MasteringLinux Shell Scripting	Andrew Mallett	Packt Publishing	1/e, 2015

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	The Linux Command Line	The Linux Command Line	The Linux Command Line	The Linux Command Line
2	William E. Shotts, Jr.	William E. Shotts, Jr.	William E. Shotts, Jr.	William E. Shotts, Jr.
3	Creative Commons	Creative Commons	Creative Commons	Creative Commons
4	2e/2013	2e/2013	2e/2013	2e/2013

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106113/
2	https://archive.nptel.ac.in/courses/117/106/117106113/
3	https://archive.nptel.ac.in/courses/117/106/117106113/
4	https://archive.nptel.ac.in/courses/117/106/117106113/

SEMESTER S4

COMPOUND SEMICONDUCTORS

Course Code	PEEVT413	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. Develop fundamental knowledge of compound semiconductor materials and its applications
2. Develop a strong theoretical background to understand, design and analyse devices made of compound semiconductors
3. Learn the basics of VLSI fabrication technology for compound semiconductor devices.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Compound Semiconductors: Classification of compound semiconductors- Binary, Ternary, Quaternary compound semiconductors (an overview) Material properties of compound semiconductors- Properties of III-V Compound semiconductors (GaAs, GaN, InP, AlGaAs, AlGaN, InGaAs, InAlGaN), IV Compounds: SiC, SiGe; Effect of mole fraction on bandgap and lattice constant Gallium Arsenide: Energy band structure, Crystal structure of GaAs, Velocity Field relationship III-Nitride semiconductors: Crystal structure of nitrides, Electrical and optical properties AlGaN alloy, InGaN alloy, InAlGaN quaternary alloy, Polarization Effects in nitrides: Spontaneous polarization, Piezoelectric polarization Metal semiconductor junctions: Schottky contacts, I-V characteristics of Schottky barrier junctions, Ohmic contacts Heterojunctions: Type I and Type II and Type III band alignments,	9

	Electrostatic characteristics of p-n hetero junctions: Band diagrams	
2	High Speed Devices: High speed performance parameters of devices - Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature Heterojunction Bipolar Transistors- Principle of operation, Energy band diagrams, Types of HBTs- III-V semiconductor, SiGe HBT- Structure, Band gap engineering Metal Semiconductor Field Effect Transistor (MESFET) - Structure of GaAs MESFET, Pinch off and threshold voltage, MESFET Operation and I-V characteristics, Schokley's model, Effects of velocity saturation and velocity field effects High Electron Mobility Transistors (HEMT)- GaAs HEMT- Structure of GaAs HEMT, Principle of operation, Energy band diagrams, Off voltage, I-V characteristics	9
3	Optoelectronics Devices Optical Detectors: Photodetectors- Basic principle of operation, Photodetector structures, Photodetector materials, Photodetector parameters- Responsivity and efficiency, photodetector gain; Photodiodes: p-n photodiodes- Device structure, Operation, Analysis; p-i-n photodiodes: Device Structure, Principle of operation; Avalanche photodiodes: Device Structure, Operation Principle Optical Sources: LEDs: Principle of operation of homojunction and heterojunction LEDs, LED materials; LASER: Physics of LASER, LASER materials, Fabry Perot cavity LASER	9
4	Fabrication Technology: Crystal growth, Epitaxy - Vapour phase epitaxy, Oxidation- Dry and wet oxidation, Kinetics of oxidation, Diffusion and Ion implantation, Lithographic techniques- Photolithography, Etching- Dry etching, Wet etching, Deposition techniques- Chemical vapour deposition (CVD), Metallization techniques- Evaporation and sputtering	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Summarize the various compound semiconductors and acquire knowledge of different types of junctions involved in compound semiconductor based devices	K2
CO2	Identify the important performance parameters of high speed electronic devices and in depth understanding of various high speed compound semiconductor devices	K4
CO3	Understand the physics of important optoelectronic devices made of compound semiconductors and their performance parameters	K3
CO4	Identify the important fabrication and processing technologies of compound semiconductor materials and related devices	K2

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**											
CO2	**3**			**2**	**2**							
CO3	**3**			**2**	**2**							**2**
CO4	**3**			**2**	**2**							**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Compound Semiconductor Device Physics,	Sandip Tiwari	Academic Press	(1991), ISBN 0-12-691740-X.
2	High Speed Semiconductor Devices	S.M. Sze	Wiley	(1990) ISBN 0-471-62307-5
3	VLSI fabrication principles: silicon and gallium arsenide.	Ghandhi, Sorab K	John Wiley & Sons, 1994.	1994.
4	Fundamentals of semiconductor devices.	Achuthan, M. K., and MK Achuthan KN Bhat	Tata McGraw-Hill,	2006.
5	Semiconductor devices for high-speed optoelectronics. Vol. 116. Cambridge:	Ghione, Giovanni	Cambridge University Press	2009.
6	Physics of Semiconductor Devices	S. M. Sze, Kwok K. Ng.	John Wiley& Sons	Third Edition
7	Lectures on "High speed devices and circuits"	K. N. Bhat	NPTEL Course.	
8	Nitride Semiconductor Devices" Fundamentals and Applications	Hadis MorkoSc	Wiley VCH Verlag GMBH & Co. KGaA.	
9	Power GaN Devices" (pp. 299-300).	Meneghini, M., Meneghesso, G. & Zanoni, E.	Berlin: Springer.	(2017).
10	Lectures on "VLSI Technology" by, NPTEL Course.	Dr. Nanditha Das Gupta	NPTEL Course.	

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Solid State Electronic Devices	Ben G. Streetman and Sanjay Kumar Banerjee	Pearson	6/e, 2010
2	Semiconductor Physics and Devices; Basic Principles,	Donald E Neamen	McGraw-Hill	Third Edition, 2003

SEMESTER S4

COMPUTER NETWORKS

Course Code	PEEVT414	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To give the basic concepts of computer network and working of layers, protocols and interfaces in a computer network.
2. To introduce the fundamental techniques used in implementing secure network communications and give them an understanding of common threats and its defences.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to computer communication:** Transmission modes, asynchronous, synchronous, simplex, half duplex, full duplex communication. Switching Network criteria, physical structures, network models, categories of networks, Interconnection of Networks Network models, OSI model, TCP/IP protocol suite.	9
2	**Physical layer:** Guided and unguided transmission media **Data Link Layer**: Framing, Flow control (stop and wait , sliding window flow control) Error control, Error detection(check sum, CRC), Bit stuffing, Ethernet (802.3), CSMA/CD, Logical link control, Wireless LAN (802.11), CSMA/CA	9
3	**Network Layer:** Routing and Forwarding, Static routing and Dynamic routing, IPv4 & IPV6, Address Resolution protocols (ARP, RARP) Routing Algorithms: Distance vector routing algorithm, Routing Protocols: Routing Information protocol (RIP), Networking devices - Hubs, Bridges & Switches **Transport Layer:** UDP, TCP, Congestion Control & Quality of Service –	9

	Data traffic. **Application Layer**: Introduction	
4	Information security: common attacks Security at Application Layer (E-MAIL, PGP and S/MIME). Security at Transport Layer (SSL and TLS). Security at Network Layer (IPSec). Firewalls, limitations of firewalls,	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Summarize the principles and components of computer networks, switching, and the layered network architecture.	**K2**
CO2	Demonstrate protocols and the functions of different layers.	**K2**
CO3	Analyse the concept of routing and addressing protocols in the context of computer networking	**K3**
CO4	Outline the basic concepts of information security at different layers of computer networks.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3											2
CO2	3											2
CO3	3	2	2	2								2
CO4	3	3	2	2								2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Computer Network A Top-down Approach Featuring the Internet	J F Kurose and K W Ross	Pearson Education	3/e, 2010
2	Cryptography & Network Security	Behrouz A. Forouzan	Tata McGraw-HillQ	IV Edition,2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Data Communications and Networking	Behrouz A. Forouzan	Tata McGraw-HillQ	IV Edition,2006
2	Computer Network- A System Approach	Larry Peterson and Bruce S Davie	Elsevier India	IV Edition,2011

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/O--rkQNKqls?si=ChlxAJyFFuJvPUWc
2	https://youtu.be/rGWPOm3ectk?si=4fJ24XFXyAXL9hWo
3	https://youtu.be/5vbPS-KnhvI?si=oRj_WZ209CZQTzhv
4	https://youtu.be/P1uAtSaHfHU?si=EFfnahZex4BFfbZG

SEMESTER S4

ECONOMICS FOR ENGINEERS

Course Code	UCHUT346	CIE Marks	50
Teaching Hours/Week (L: T:P: R)	2:0:0:0	ESE Marks	50
Credits	2	Exam Hours	2 Hrs.30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. Understanding of finance and costing for engineering operation, budgetary planning and control
2. Provide fundamental concept of micro and macroeconomics related to engineering industry
3. Deliver the basic concepts of Value Engineering.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Basic Economics Concepts - Basic economic problems – Production Possibility Curve – Utility – Law of diminishing marginal utility – Law of Demand - Law of supply – Elasticity - measurement of elasticity and its applications – Equilibrium- Changes in demand and supply and its effects Production function - Law of variable proportion – Economies of Scale – Internal and External Economies – Cobb-Douglas Production Function	6
2	Cost concepts – Social cost, private cost – Explicit and implicit cost – Sunk cost - Opportunity cost - short run cost curves - Revenue concepts Firms and their objectives – Types of firms – Markets - Perfect Competition – Monopoly - Monopolistic Competition - Oligopoly (features and equilibrium of a firm)	6
3	Monetary System – Money – Functions - Central Banking –Inflation - Causes and Effects – Measures to Control Inflation - Monetary and Fiscal policies – Deflation Taxation – Direct and Indirect taxes (merits and demerits) - GST	6

	National income – Concepts - Circular Flow – Methods of Estimation and Difficulties - Stock Market – Functions- Problems faced by the Indian stock market-Demat Account and Trading Account – Stock market Indicators- SENSEX and NIFTY	
4	Value Analysis and value Engineering - Cost Value, Exchange Value, Use Value, Esteem Value - Aims, Advantages and Application areas of Value Engineering - Value Engineering Procedure - Break-even Analysis - Cost-Benefit Analysis - Capital Budgeting - Process planning	**6**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Case Study/Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the fundamentals of various economic issues using laws and learn the concepts of demand, supply, elasticity and production function.	**K2**
CO2	Develop decision making capability by applying concepts relating to costs and revenue, and acquire knowledge regarding the functioning of firms in different market situations.	**K3**
CO3	Outline the macroeconomic principles of monetary and fiscal systems, national income and stock market.	**K2**
CO4	Make use of the possibilities of value analysis and engineering, and solve simple business problems using break even analysis, cost benefit analysis and capital budgeting techniques.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	-	-	-	-	-	1	-	-	-	-	1	-
CO2	-	-	-	-	-	1	1	-	-	-	1	-
CO3	-	-	-	-	1	-	-	-	-	-	2	-
CO4	-	-	-	-	1	1	-	-	-	-	2	-

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Managerial Economics	Geetika, Piyali Ghosh and Chodhury	Tata McGraw Hill,	2015
2	Engineering Economy	H. G. Thuesen, W. J. Fabrycky	PHI	1966
3	Engineering Economics	R. Paneerselvam	PHI	2012

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Engineering Economy	Leland Blank P.E, Anthony Tarquin P. E.	Mc Graw Hill	7^{TH} Edition
2	Indian Financial System	Khan M. Y.	Tata McGraw Hill	2011
3	Engineering Economics and analysis	Donald G. Newman, Jerome P. Lavelle	Engg. Press, Texas	2002
4	Contemporary Engineering Economics	Chan S. Park	Prentice Hall of India Ltd	2001

SEMESTER S3/S4

ENGINEERING ETHICS AND SUSTAINABLE DEVELOPMENT

Course Code	UCHUT347	CIE Marks	50
Teaching Hours/Week (L: T:P: R)	2:0:0:0	ESE Marks	50
Credits	2	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. Equip with the knowledge and skills to make ethical decisions and implement gender-sensitive practices in their professional lives.
2. Develop a holistic and comprehensive interdisciplinary approach to understanding engineering ethics principles from a perspective of environment protection and sustainable development.
3. Develop the ability to find strategies for implementing sustainable engineering solutions.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Fundamentals of ethics** - Personal vs. professional ethics, Civic Virtue, Respect for others, **Profession and Professionalism,** Ingenuity, diligence and responsibility, Integrity in design, development, and research domains, Plagiarism, a balanced outlook on law - challenges - case studies, **Technology and digital revolution**-Data, information, and knowledge, Cybertrust and cybersecurity, Data collection & management, **High technologies: connecting people and places**-accessibility and social impacts, **Managing conflict**, Collective bargaining, **Confidentiality**, Role of confidentiality in moral integrity, **Codes of Ethics**. **Basic concepts in Gender Studies** - sex, gender, sexuality, gender spectrum: beyond the binary, gender identity, gender expression, gender stereotypes, **Gender disparity and discrimination in education**,	6

	employment and everyday life, History of women in Science & Technology, Gendered technologies & innovations**, Ethical values and practices in connection with gender** - equity, diversity & gender justice, **Gender policy and women/transgender empowerment initiatives.**	
2	**Introduction to Environmental Ethics:** Definition, importance and historical development of environmental ethics, key philosophical theories (anthropocentrism, biocentrism, ecocentrism). **Sustainable Engineering Principles:** Definition and scope, triple bottom line (economic, social and environmental sustainability), life cycle analysis and sustainability metrics. **Ecosystems and Biodiversity:** Basics of ecosystems and their functions, Importance of biodiversity and its conservation, Human impact on ecosystems and biodiversity loss, An overview of various ecosystems in Kerala/India, and its significance. **Landscape and Urban Ecology:** Principles of landscape ecology, Urbanization and its environmental impact, Sustainable urban planning and green infrastructure.	**6**
3	**Hydrology and Water Management:** Basics of hydrology and water cycle, Water scarcity and pollution issues, Sustainable water management practices, Environmental flow, disruptions and disasters. **Zero Waste Concepts and Practices:** Definition of zero waste and its principles, Strategies for waste reduction, reuse, reduce and recycling, Case studies of successful zero waste initiatives. **Circular Economy and Degrowth:** Introduction to the circular economy model, Differences between linear and circular economies, degrowth principles, Strategies for implementing circular economy practices and degrowth principles in engineering. **Mobility and Sustainable Transportation:** Impacts of transportation on the environment and climate, Basic tenets of a Sustainable Transportation design, Sustainable urban mobility solutions, Integrated mobility systems, E-Mobility, Existing and upcoming models of sustainable mobility solutions.	**6**
4	**Renewable Energy and Sustainable Technologies:** Overview of renewable energy sources (solar, wind, hydro, biomass), Sustainable technologies in energy production and consumption, Challenges and opportunities in renewable energy adoption. **Climate Change and Engineering Solutions:** Basics of climate change science, Impact of climate change on natural and human systems, Kerala/India and the Climate crisis, Engineering solutions to mitigate, adapt and build resilience to climate change. **Environmental**	**6**

	Policies and Regulations: Overview of key environmental policies and regulations (national and international), Role of engineers in policy implementation and compliance, Ethical considerations in environmental policy-making. **Case Studies and Future Directions:** Analysis of real-world case studies, Emerging trends and future directions in environmental ethics and sustainability, Discussion on the role of engineers in promoting a sustainable future.	

Course Assessment Method
(CIE: 50 marks , ESE: 50)

Continuous Internal Evaluation Marks (CIE):

Continuous internal evaluation will be based on individual and group activities undertaken throughout the course and the portfolio created documenting their work and learning. The portfolio will include reflections, project reports, case studies, and all other relevant materials.

- The students should be grouped into groups of size 4 to 6 at the beginning of the semester. These groups can be the same ones they have formed in the previous semester.
- Activities are to be distributed between 2 class hours and 3 Self-study hours.
- The portfolio and reflective journal should be carried forward and displayed during the 7th Semester Seminar course as a part of the experience sharing regarding the skills developed through various courses.

Sl. No.	Item	Particulars	Group/ Individual (G/I)	Marks
1	Reflective Journal	Weekly entries reflecting on what was learned, personal insights, and how it can be applied to local contexts.	I	5
2	Micro project (Detailed documentation of the project, including methodologies, findings, and reflections)	1 a) Perform an Engineering Ethics Case Study analysis and prepare a report 1 b) Conduct a literature survey on 'Code of Ethics for Engineers' and prepare a sample code of ethics	G	8
		2. Listen to a TED talk on a Gender-related topic, do a literature survey on that topic and make a report citing the relevant papers with a specific analysis of the Kerala context	G	5
		3. Undertake a project study based on the concepts of sustainable development* - Module II, Module III & Module IV	G	12
3	Activities	2. One activity* each from Module II, Module III & Module IV	G	15
4	Final Presentation	A comprehensive presentation summarising the key takeaways from the course, personal reflections, and proposed future actions based on the learnings.	G	5
		Total Marks		**50**

*Can be taken from the given sample activities/projects

Evaluation Criteria:

- **Depth of Analysis**: Quality and depth of reflections and analysis in project reports and case studies.
- **Application of Concepts**: Ability to apply course concepts to real-world problems and local contexts.
- **Creativity**: Innovative approaches and creative solutions proposed in projects and reflections.
- **Presentation Skills**: Clarity, coherence, and professionalism in the final presentation.

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Develop the ability to apply the principles of engineering ethics in their professional life.	**K3**
CO2	Develop the ability to exercise gender-sensitive practices in their professional lives	**K4**
CO3	Develop the ability to explore contemporary environmental issues and sustainable practices.	**K5**
CO4	Develop the ability to analyse the role of engineers in promoting sustainability and climate resilience.	**K4**
CO5	Develop interest and skills in addressing pertinent environmental and climate-related challenges through a sustainable engineering approach.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1						3	2	3	3	2		2
CO2		1				3	2	3	3	2		2
CO3						3	3	2	3	2		2
CO4		1				3	3	2	3	2		2
CO5						3	3	2	3	2		2

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Ethics in Engineering Practice and Research	Caroline Whitbeck	Cambridge University Press & Assessment	2nd edition & August 2011
2	Virtue Ethics and Professional Roles	Justin Oakley	Cambridge University Press & Assessment	November 2006
3	Sustainability Science	Bert J. M. de Vries	Cambridge University Press & Assessment	2nd edition & December 2023
4	Sustainable Engineering Principles and Practice	Bhavik R. Bakshi,	Cambridge University Press & Assessmen	2019
5	Engineering Ethics	M Govindarajan, S Natarajan and V S Senthil Kumar	PHI Learning Private Ltd, New Delhi	2012
6	Professional ethics and human values	RS Naagarazan	New age international (P) limited New Delhi	2006.
7	Ethics in Engineering	Mike W Martin and Roland Schinzinger,	Tata McGraw Hill Publishing Company Pvt Ltd, New Delhi	4" edition, 2014

Suggested Activities/Projects:

Module-II

- Write a reflection on a local environmental issue (e.g., plastic waste in Kerala backwaters or oceans) from different ethical perspectives (anthropocentric, biocentric, ecocentric).
- Write a life cycle analysis report of a common product used in Kerala (e.g., a coconut, bamboo or rubber-based product) and present findings on its sustainability.
- Create a sustainability report for a local business, assessing its environmental, social, and economic impacts
- Presentation on biodiversity in a nearby area (e.g., a local park, a wetland, mangroves, college campus etc) and propose conservation strategies to protect it.
- Develop a conservation plan for an endangered species found in Kerala.
- Analyze the green spaces in a local urban area and propose a plan to enhance urban ecology using native plants and sustainable design.
- Create a model of a sustainable urban landscape for a chosen locality in Kerala.

Module-III

- Study a local water body (e.g., a river or lake) for signs of pollution or natural flow disruption and suggest sustainable management and restoration practices.
- Analyse the effectiveness of water management in the college campus and propose improvements - calculate the water footprint, how to reduce the footprint, how to increase supply through rainwater harvesting, and how to decrease the supply-demand ratio
- Implement a zero waste initiative on the college campus for one week and document the challenges and outcomes.
- Develop a waste audit report for the campus. Suggest a plan for a zero-waste approach.
- Create a circular economy model for a common product used in Kerala (e.g., coconut oil, cloth etc).
- Design a product or service based on circular economy and degrowth principles and present a business plan.
- Develop a plan to improve pedestrian and cycling infrastructure in a chosen locality in Kerala

Module-IV

- Evaluate the potential for installing solar panels on the college campus including cost-benefit analysis and feasibility study.
- Analyse the energy consumption patterns of the college campus and propose sustainable alternatives to reduce consumption - What gadgets are being used? How can we reduce demand using energy-saving gadgets?
- Analyse a local infrastructure project for its climate resilience and suggest improvements.
- Analyse a specific environmental regulation in India (e.g., Coastal Regulation Zone) and its impact on local communities and ecosystems.
- Research and present a case study of a successful sustainable engineering project in Kerala/India (e.g., sustainable building design, water management project, infrastructure project).
- Research and present a case study of an unsustainable engineering project in Kerala/India highlighting design and implementation faults and possible corrections/alternatives (e.g., a housing complex with water logging, a water management project causing frequent floods, infrastructure project that affects surrounding landscapes or ecosystems).

SEMESTER S4

LINEAR INTEGRATED CIRCUITS LAB

Course Code	PCECL407	CIE Marks	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	ESE Marks	50
Credits	2	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Lab

Course Objectives:

1. To study the design and implementation of various Linear Integrated Circuits.
2. To familiarize the simulation of basic Linear Integrated Circuits...

Details of Experiment

Expt. No	Experiments
	Part A – List of Experiments using Op Amps (Minimum seven experiments mandatory)
1	Familiarization of Operational amplifiers - Inverting and Non inverting amplifiers, Integrator, Differentiator - frequency response, Adder, Comparators
2	Measurement of Op-Amp parameters
3	Difference Amplifier and Instrumentation amplifier
4	Schmitt trigger circuit
5	Astable and Monostable multivibrators
6	Waveform generators using Op Amps - Triangular and Sawtooth
7	Wien bridge oscillator - without & with amplitude stabilization
8	RC Phase shift Oscillator
9	Active first and second order filters (LPF, HPF, BPF and BRF)
10	Active Notch filter to eliminate the 50Hz power line frequency
11	Precision rectifiers
Expt. No	**Part B – Application circuits using ICs [Minimum three experiments are to be done]**
1	Astable and Monostable multivibrator using Timer IC NE555

2	DC power supply using IC 723: Low voltage and high voltage configurations, Short circuit and Fold-back protection.
3	A/D converters- counter ramp and flash type.
4	D/A Converters - R-2R ladder circuit
5	Study of PLL IC: free running, frequency lock range and capture range
Expt No.	**Part C – Simulation experiments** **[**The experiments shall be conducted using open tools such as QUCS, KiCad or variants of SPICE]
1	Simulation of any three circuits from experiments 3, 5, 6, 7, 8, 9, 10 and 11 of section I
2	Simulation of experiments 3 or 4 from section II

Course Assessment Method (CIE: 50 Marks, ESE 50 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work, experiments, Viva and Timely completion of Lab Reports / Record. (Continuous Assessment)	Internal Exam	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voice	Record	Total
10	**15**	**10**	**10**	**5**	**50**

Mandatory requirements for ESE:

1. Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.
2. Endorsement by External Examiner: The external examiner shall endorse the record.

Course Outcomes (COs)

At the end of the course the student will be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design and implement basic linear integrated circuits using Op Amps.	**K4**
CO2	Design and implement basic linear integrated circuits using linear ICs.	**K4**
CO3	Design and simulate the functioning of basic linear integrated circuits and linear ICs. using simulation tools.	**K4**
CO4	Effectively troubleshoot a given circuit and analyze it	**K4**

K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2						3			3
CO2	3	3	2						3			3
CO3	3	3	2		3				3			3
CO4	3	3	2						3			3

1: Slight (Low),2: Moderate (Medium),3: Substantial (High), : No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Linear Integrated Circuits	D. Roy Choudhary and Shail B Jain	New Age International Private Limited	6th edition, 2021
2	Introduction to Pspice Using Orcad for Circuits and Electronics	M. H. Rashid	Pearson	3rd edition, 2015

Continuous Assessment (25 Marks)

1. **Preparation and Pre-Lab Work (7 Marks)**

    - Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
    - Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. **Conduct of Experiments (7 Marks)**

    - Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
    - Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
    - Teamwork: Collaboration and participation in group experiments.

3. **Lab Reports and Record Keeping (6 Marks)**

    - Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
    - Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

    - Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

    - Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
    - Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.

- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
- Creativity and logic in algorithm or experimental design.

2. Conduct of Experiment/Execution of Work/Programming (15 Marks)

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. Result with Valid Inference/Quality of Output (10 Marks)

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. Viva Voce (10 Marks)

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. Record (5 Marks)

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER S4

MICROCONTROLLERS LAB

Course Code	**PCECL408**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCECL307-Logic Circuit Design and Simulation Lab	**Course Type**	Lab

Course Objectives:

1. To learn Microcontroller Programming using Assembly and C language
2. To learn Microcontroller interfaces to various modules
3. To learn any advanced microcontrollers like ARM or higher.
4. To learn Embedded System Design

Expt. No	Experiment
	PART A – Data manipulation experiments using Assembly language(Min 4 has to be completed)
1	Multiplication of two 16-bit numbers.
2	Largest/smallest from a series.
3	Sorting (Ascending/Descending) of data.
4	Matrix addition.
5	LCM and HCF of two 8-bit numbers.
6	Code conversion – Hex to Decimal/ASCII to Decimal and vice versa.
	PART B - Interface to Microcontroller Assembly/C language (Min 3 has to be completed)
1.	Time delay generation and relay interface.
2.	Display (LED/Seven segments/LCD) and keyboard interface.
3.	ADC interface.
4.	DAC interface with waveform generation.
5.	Stepper motor and DC motor interface.
	PART C - Interface with Advanced Microcontroller using C language (Min 3 has to be completed)
1.	PWM generation for DC motor control.
2.	Object/Visitor Counter.

3.	UART interface to Bluetooth.
4.	SPI/I2C interface to display.
5.	Real-time clock.

Course Assessment Method (CIE: 50 Marks, ESE 50 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work, experiments, Viva and Timely completion of Lab Reports / Record. (Continuous Assessment)	Internal Exam	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voice	Record	Total
10	**15**	**10**	**10**	**5**	**50**

Mandatory requirements for ESE:

- Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.
- Endorsement by External Examiner: The external examiner shall endorse the record.

Course Outcomes (COs)

At the end of the course the student will be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Develop 8051 Microcontroller programs	**K5**
CO2	Design and implement various interfaces to the 8051 Microcontroller	**K6**
CO3	Design and implement an Embedded System using a 8051 microcontroller	**K6**
CO4	Design and implement an Embedded System using an ARM processor	**K6**

K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	2								2
CO2	3	3	3	2	3			2				2
CO3	3	3	3	3	3	3	3	3	3	3	3	3
CO4	3	3	3	3	3	3	3	3	3	3	3	3

1: Slight (Low),2: Moderate (Medium),3: Substantial (High), : No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	The 8051 Microcontroller and Embedded Systems Using Assembly and C	Muhammad Ali Mazidi Janice Gillispie Mazidi Rolin D. McKinlay	Printice Hall -Inc	Second, 2007
2	The 8051 Microcontroller Architecture, Programming and Applications	Kenneth J Ayala Dhananjay V Gadre	Cengage Learning	2010

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	8051 Hardware Description	Datasheet	Intel Corporation	1992
2	Microprocessors and Microcontrollers	Lyla B. Das	Pearson Education	2011
3	ARM System-on-Chip Architecture	Steve Furber	Addison-Wesley Educational Publishers Inc	2000
4	System-on-Chip Design with Arm(R) Cortex(R)-M Processors	Joseph Yiu	ARM Education Media	2019

Video Links (NPTEL, SWAYAM…)	
Sl. No.	**Link ID**
1	Microprocessors and Microcontrollers - https://nptel.ac.in/courses/106108100
2	Microcontrollers and Applications - https://nptel.ac.in/courses/117104072
3	Embedded System Design With ARM - https://onlinecourses.nptel.ac.in/noc22_cs93

Continuous Assessment (25 Marks)

1. **Preparation and Pre-Lab Work (7 Marks)**

   - Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
   - Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. **Conduct of Experiments (7 Marks)**

   - Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
   - Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
   - Teamwork: Collaboration and participation in group experiments.

3. **Lab Reports and Record Keeping (6 Marks)**

   - Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
   - Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

   - Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

    - Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
    - Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
    - Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
    - Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

    - Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. **Result with Valid Inference/Quality of Output (10 Marks)**

    - Accuracy of Results: Precision and correctness of the obtained results.
    - Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. **Viva Voce (10 Marks)**

    - Ability to explain the experiment, procedure results and answer related questions
    - Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. **Record (5 Marks)**

    - Completeness, clarity, and accuracy of the lab record submitted.

SEMESTER 5

Electronics Engineering (VLSI Design and Technology)

SEMESTER S5

DIGITAL CMOS DESIGN

Course Code	**PCEVT501**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-1-0-0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. This Course aims to offer distinctive coverage of the dynamic and static circuits and to discuss important aspects of timing and synchronisation, power dissipation, interconnect packing, and signal integrity in real-world system design

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**MOS TRANSISTOR PRINCIPLES** Introduction to CMOS technology: CMOS logic, CMOS fabrication and layout, Design partitioning, Circuit design, Physical Design, Design verification, Fabrication, Packaging and testing. **MOS transistor**: MOS Transistor Basics, Secondary Effects, Process Variations, Technology Scaling.	11
2	**Static and Dynamic circuits:** **CMOS Inverter:** Static CMOS Inverter: DC Characteristics, Beta Ratio Effects, Noise margin. Other static CMOS logic gates, static properties (2 input NAND, NOR), Combinational logic circuits. **Fundamentals of dynamic logic**: Dynamic pass transistor circuits, High performance dynamic circuits-Domino CMOS, Multi Output Domino Logic, Dual-rail Domino Logic, NP Domino logic (NORA) logic.	11
3	**Designing arithmetic building blocks:** Adders: Design considerations, Fast adders, Multipliers, Barrel Shifters, Speed and Area Trade-offs. **Semiconductor Memories**: Memory Design, SRAM, DRAM structure and	11

	implementations	
4	**Interconnect effects**: Introduction, Wire Geometry, Interconnect Modelling: Resistance, Capacitance, and Inductance. Interconnect Impact: Delay, Energy, Crosstalk, Inductive Effects, Effective Resistance and Elmore Delay.	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
● 2 Questions from each module. ● Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	● Each question carries 9 marks. ● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the basics of MOS Transistors and CMOS Inverter.	**K2**
CO2	Design Static and Dynamic Logic circuits.	**K3**
CO3	Design arithmetic and logic circuits and memory elements.	**K3**
CO4	Simulate and calculate the impacts of R, L, and C parasitic, the effects of technological scaling, ways to deal with capacitive crosstalk, calculate the RC delay, and inductive effects.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**										
CO2	**3**	**3**										
CO3	**3**	**3**	**2**									
CO4	**3**	**3**										

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Integrated Circuit Design	Neil H. E. Weste and David Money Harris	Pearson Education.	4/e, 2011
2	CMOS Digital Integrated Circuits	Sung-Mo Kang, Yusuf Leblebici	Tata McGraw-Hill Education	3/e, 2003
3	Digital Integrated Circuits – A Design Perspective	Rabaey, Chandrakasan and Nikolic	Pearson Education.	2/e

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS, Circuit Design, Layout, and Simulation	R. Jacob Baker, Harry W. Li, David E. Boyce	Wiley Interscience	3/e
2	Introduction to VLSI Circuits and Systems	John P. Uyemura	John Wiley & Sons, Inc.	

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc22_ee08/preview, https://nptel.ac.in/courses/117103066,
2	https://onlinecourses.nptel.ac.in/noc22_ee08/preview
3	https://www.youtube.com/watch?v=8LRMqA5ZPss, https://archive.nptel.ac.in/courses/117/101/117101058/
4	https://archive.nptel.ac.in/courses/117/103/117103066/

SEMESTER S5

FPGA BASED SYSTEM DESIGN

Course Code	PCEVT502	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. This Course aims to inculcate the knowledge on advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of the system design. The course would enable the students to apply their knowledge for the design of advanced digital hardware systems with the help of FPGA tools.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**VERILOG HDL** :Verilog HDL Coding Style: Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - System Tasks & Compiler Directives - Test Bench - Data Flow Modeling - Behavioral level Modeling - Tasks & Functions	11
2	**FPGA ARCHITECTURE**: FPGA Architectural options, coarse vs fine grained, vendor specific issues (emphasis on Xilinx FPGA), Antifuse, SRAM and EPROM based FPGAs, FPGA logic cells, Interconnection network and I/O Pad	11
3	**VERILOG MODELLING** :Verilog Modelling of Combinational and Sequential Circuits: Behavioral, Data Flow and Structural Realization – Adders – Multipliers- Comparators - Flip Flops - Realization of Shift Register - Realization of a Counter- Synchronous and Asynchronous FIFO –Single port and Dual port RAM – Pseudo Random LFSR – Cyclic Redundancy Check	11
4	**XILLINX** :System Design Examples using Xillinx FPGAs – Traffic light Controller, Real Time Clock - Interfacing using FPGA: Keyboard, LCD **Commercial FPGAs:** Xilinx, Altera, Actel (Different series description only)	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand complex combinational and sequential digital circuits.	**K2**
CO2	Apply Verilog HDL in modelling Combinational and sequential digital circuits	**K3**
CO3	Understand digital circuits with Verilog HDL at behavioural, structural, and RTL Levels	**K2**
CO4	Understand the FPGA Architecture and implement the combinational and sequential digital circuits in FPGA	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**		**1**									**2**
CO2	**2**		**2**									**2**
CO3	**3**	**2**	**3**		**1**							**2**
CO4				**1**								**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	FPGA Prototyping by Verilog Examples	Pong P. Chu	John Wiley & Sons	2008
2	Verilog HDL: A Guide to Digital Design and Synthesis	Samir Palnitkar	Prentice Hall PTR	Second Edition,2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Application Specific Integrated Circuits	M.J.S. Smith	Pearson	2000
2	Digital Design using VHDL	Peter Ashenden	Elsevier	2007
3	FPGA based system design	W. Wolf	Pearson	2004

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/IXjNLK7GC70
2	https://youtu.be/vHLBO05TeyU?si=uef41ETWM7t95oiL

SEMESTER S5

VLSI TECHNOLOGY

Course Code	**PCEVT503**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCECT302	**Course Type**	Theory

Course Objectives:

1. To give knowledge about IC fabrication techniques and VLSI design methodologies.
2. To impart the skill of analysis and design of MOSFET and CMOS logic circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Material Preparation- Purification, Crystal growth (CZ process), wafer preparation. Thermal Oxidation- Dry and Wet oxidation, Diffusion- diffusion techniques. Ion implantation -Technique, annealing. Epitaxy: Vapour phase epitaxy and molecular beam epitaxy Lithography- Photo lithographic sequence, Electron Beam Lithography. Etching and metal deposition, CMOS Twin well process	9
2	Moore's law. ASIC design, Full custom ASICs, Standard cell based ASICs, Gate array based ASICs, SoCs, FPGA devices, ASIC and FPGA Design flows, Top-Down and Bottom-Up design methodologies. Logical and Physical design. Speed power and area considerations in VLSI design	9
3	CMOS inverters- DC characteristics, switching characteristics, power dissipation , Layout Design rules, Stick Diagram and layout of CMOS Inverter, two input NAND and NOR gates.	9

	MOSFET Logic Design -Pass transistor logic, Complementary pass transistor logic and transmission gate logic , realization of functions	
4	Read Only Memory-4x4 MOS ROM Cell arrays(OR,NOR,NAND) Random Access Memory –SRAM-Six transistor CMOS SRAM cell, DRAM –Three transistor and One transistor Dynamic Memory Cell	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Summarize MOSFET fabrication techniques	**K2**
CO2	Outline the various methodologies in ASIC and FPGA design.	**K2**
CO3	Understand CMOS technology.	**K2**
CO4	Design VLSI Logic circuits with various MOSFET logic families.	**K2**
CO5	Compare different types of memory elements	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**											**3**
CO2	**2**											**3**
CO3	**2**	**2**	**2**		**2**							**3**
CO4	**2**	**2**	**2**		**2**							**3**
CO5	**2**											**3**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introduction to VLSI Circuits and Systems,	John P Uyemura,	Wiley India,	2006
2	VLSI Technology	S.M. SZE	McGraw-Hill	Indian Edition,2/e,,2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Integrated Circuits- A Design Perspective	Jan M. Rabaey	Prentice Hall	Second Edition, 2005
2	Principles of CMOS VLSI Design-A Systems Perspective	Neil H.E. Weste , Kamran Eshraghian	Pearson Publication	Second Edition,2005
3	Design of Analog CMOS Integrated Circuits	Razavi	McGraw Hill Education India Education, New Delhi	1e,2003.
4	CMOS Digital Integrated Circuits- Analysis & Design	Sung –Mo Kang & Yusuf Leblebici,	McGraw-Hill,	Third Ed., 2003.
5	Fundamentals of Modern VLSI Devices	Yuan Taur & Ning,	Cambridge University Press,	2008

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/Iv4Cj2A3ldw?si=8wkrFXV583vMiJDh, https://youtu.be/fokSc0xlTfM?si=pbWd_UtVbvVacPA,
2	https://youtu.be/oZSv68esbgI?si=AoGIe2JX9G6GsdYZ, https://youtu.be/4cPkr1VHu7Q?si=alAxpL5vUn9s24zX, https://youtu.be/ht7nEjNydDU?si=_E7m1qMrUvqdcya4
3	https://youtu.be/UuafwIJAKhY?si=PRrPHzB4mWxwm5h7
4	https://youtu.be/Y8FvvzcocT4?si=3anWLYD00aACws9y

SEMESTER S5

EMBEDDED SYSTEM DESIGN

Course Code	PBEVT504	CIE Marks	60
Teaching Hours/Week (L: T:P: R)	3:0:0:1	ESE Marks	40
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304, PBECT404	Course Type	Theory

Course Objectives:

1. To design an embedded electronic circuit and implement the same
2. To develop system using ARM processor and its peripherals
3. Implement and maintain applications written in Embedded C

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**1.1 Complex Systems and Microprocessors** Embedding Computers, Characteristics of Embedded Computing Applications, Application of Microprocessors, The Physics of Software, Challenges in Embedded Computing System, Characteristics and quality attributes of an embedded system, Performance in Embedded Computing **1.2 The Embedded System Design Process** Requirements, Specification, Architecture Design, Designing Hardware and Software Components, System Integration. **1.3 Formalisms for System Design** Structural Description, Behavioral Description, An embedded system design example. **1.4 Embedded product development cycle (EDLC)** Different phases of EDLC, EDLC models	**10**
2	**2.1 Communication devices** Serial Communication Standards and Devices - UART, HDLC and SPI. Serial Bus Protocols - I2C Bus, CAN Bus and USB Bus. Parallel communication standards ISA, PCI and PCI-X Bus.	**10**

	2.2 Memory Memory devices and systems – ROM-Flash, EEPROM,RAM-SRAM, DRAM, Cache memory, memory mapping and addresses, memory management unit– DMA . **2.3 Interrupts/Device Driver** Interrupts--Interrupt sources, recognizing an interrupt, ISR – Device drivers for handling ISR, Interrupt latency.	
3	**3.1 ARM Processor architecture** The Acorn RISC Machine, Architectural inheritance, The ARM programmer's model, ARM development tools. **3.2 ARM Assembly Language Programming** Data processing instructions, Data transfer instructions, Control flow instructions, writing simple assembly language programs. **3.3 ARM Organization and Implementation** Three stage pipeline ARM organization, five stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface	**10**
4	**4.1 Architectural Support for High-Level Languages** Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Assembly and C language programming applications of embedded systems. **4.2 Architectural Support for System Development** The ARM memory interface, The Advanced Microcontroller Bus Architecture (AMBA). **4.3 Operating system basics** Functions of OS, Kernel, types of operating systems. **4.4Introduction to Real time operating systems** Tasks, process, threads, multiprocessing and multitasking, task scheduling, task communication, choosing an RTOS	**10**

Suggestion on Project Topics

1. Design and Implementation of ARM Cortex Based Motor Speed Control
2. ARM7 Processor based Auto Ignition control in automobiles
3. ARM Processor-based Real-time Car Theft Detection
4. Automated Irrigation system using ARM processor
5. ARM processor based Industrial Automation using GSM/Wi-Fi

Course Assessment Method
(CIE: 60 marks, ESE: 40 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Project	Internal Ex-1	Internal Ex-2	Total
5	30	12.5	12.5	60

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 2 marks **(8x2 =16 marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 2 sub divisions. Each question carries 6 marks. **(4x6 = 24 marks)**	**40**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the embedded system fundamentals and system design	**K1**
CO2	Understand the peripheral devices and their interfacing with the processor.	**K2**
CO3	Understand the ARM processor architecture and pipeline processor organization.	**K2**
CO4	Write programs in assembly and high-level languages for ARM processor.	**K3**
CO5	Understand the basics of real time operating systems and their use in embedded systems.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**2**		**1**						**2**	**2**
CO2	**3**	**3**	**3**		**3**				**2**			**2**
CO3	**3**	**3**		**2**	**2**		**2**		**2**			**2**
CO4	**3**	**3**		**2**	**2**		**2**					**2**
CO5	**3**	**3**	**3**	**2**	**2**		**2**		**2**			**2**

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Embedded Systems Architecture, Programming and Design	Raj kamal	TMH	2nd edition,2003
2	Introduction to Embedded Systems	K.V Shibu	McGraw Hill Education India	2nd edition,2016
3	Computers as Components: Principles of Embedded Computing System Design	Wayne Wolf	Morgan Kaufman Publishers - Elsevier	3rd edition,2008
4	ARM system-on-chip architecture	Steve Furber	Addison Wesley	2nd edition,2000

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	An Embedded Software Primer	David E. Simon	Pearson Education Asia	1st Edition,2000
2	Embedded Systems Design	Steve Heath	Newnes – Elsevier	2nd Edition,2002
3	Embedded Systems Architecture, A Comprehensive Guide for Engineers and Programmers	Tammy Noergaard,	Newnes – Elsevier	2nd Edition,2012

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/108/102/108102169/
2	https://onlinecourses.nptel.ac.in/noc22_cs93/preview
3	https://archive.nptel.ac.in/courses/108/102/108102169/
4	https://archive.nptel.ac.in/courses/106/105/106105172/

PBL Course Elements

L: Lecture (3 Hrs.)	**R: Project (1 Hr.), 2 Faculty Members**		
	Tutorial	**Practical**	**Presentation**
Lecture delivery	Project identification	Simulation/ Laboratory Work/ Workshops	Presentation (Progress and Final Presentations)
Group discussion	Project Analysis	Data Collection	Evaluation
Question answer Sessions/ Brainstorming Sessions	Analytical thinking and self-learning	Testing	Project Milestone Reviews, Feedback, Project reformation (If required)
Guest Speakers (Industry Experts)	Case Study/ Field Survey Report	Prototyping	Poster Presentation/ Video Presentation: Students present their results in a 2 to 5 minutes video

Assessment and Evaluation for Project Activity

Sl. No	Evaluation for	Allotted Marks
1	Project Planning and Proposal	5
2	Contribution in Progress Presentations and Question Answer Sessions	4
3	Involvement in the project work and Team Work	3
4	Execution and Implementation	10
5	Final Presentations	5
6	Project Quality, Innovation and Creativity	3
Total		**30**

1. **Project Planning and Proposal (5 Marks)**
    - Clarity and feasibility of the project plan
    - Research and background understanding
    - Defined objectives and methodology

2. **Contribution in Progress Presentation and Question Answer Sessions (4 Marks)**
    - Individual contribution to the presentation
    - Effectiveness in answering questions and handling feedback

3. **Involvement in the Project Work and Team Work (3 Marks)**
    - Active participation and individual contribution
    - Teamwork and collaboration

4. **Execution and Implementation (10 Marks)**
    - Adherence to the project timeline and milestones
    - Application of theoretical knowledge and problem-solving
    - Final Result

5. **Final Presentation (5 Marks)**
    - Quality and clarity of the overall presentation
    - Individual contribution to the presentation
    - Effectiveness in answering questions

6. **Project Quality, Innovation, and Creativity (3 Marks)**

- Overall quality and technical excellence of the project
- Innovation and originality in the project
- Creativity in solutions and approaches

SEMESTER S5

ANALOG AND DIGITAL COMMUNICATION

Course Code	**PEEVT 521**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	GBMAT401	**Course Type**	Theory

Course Objectives:

1. This course aims to develop analog and digital communication systems

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Block diagram of a communication system. Need for modulation. Amplitude modulation, Equation and spectrum of AM signal, DSB-SC, SSB. Angle modulation: Narrow and wide band FM and their spectra, relationship between FM and PM, Carson's rule Comparison of AM and FM. Noise: external, internal, White noise.	9
2	Sampling and Quantization, Companding- A and mu-law companders. Pulse code modulation, Transmitter and receiver. DPCM transmitter and receiver. Delta modulation, Slope overload,	9
3	Baseband data transmission of digital data through AWGN channel, Mathematical model of ISI, Nyquist criterion for zero ISI, Signal modelling for ISI, Raised cosine spectrum, Vector model of AWGN channel. Matched filter and correlation receivers	9

4	Digital band pass modulation schemes-BPSK system and signal constellation. BPSK transmitter and receiver. QPSK system and Signal constellations. Plots of BER Vs SNR with analysis. QPSK transmitter and receiver. Quadrature amplitude modulation and signal constellation	9

Course Assessment Method
(CIE: 40 marks,ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Illustrate the principles of analog communication systems	**K2**
CO2	Explain the basic concepts of digital communication	**K2**
CO3	Analyse the baseband transmission of digital data through AWGN channel	**K3**
CO4	Apply various digital modulation techniques in the design of digital communication systems	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	-	-	-	2	-	-	-	-	-	-	-
CO2	3	-	-	-	2	-	-	-	-	-	-	-
CO3	3	3	3	3	2	-	-	-	-	-	-	2
CO4	3	3	3	3	2	-	-	-	-	-	-	2
CO5	3	-	-	-	2	-	-	-	-	-	-	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Communication Systems	Simon Haykin	John Wiley& Sons	4th Edition, 2015
2	Principles of Communication Systems	Herbert Taub and Donald L. Schilling	McGraw-Hill Education	4th Edition, 2013
3	Communication Systems Engineering	John G. Proakis and Masoud Salehi	Pearson	2nd Edition, 2002
4	Electronic communication systems	George Kennedy McGraw Hill 6th Edition, 2017	McGraw Hill 6th Edition, 2017	George Kennedy McGraw Hill 6th Edition, 2017
5	Digital Communications	Simon Haykin	John Wiley& Sons	4th Edition, 2015
6	Digital Communications: Fundamentals and Applications	Bernard Sklar, Pabitra Kumar Ray	Pearson	2nd Edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Modern Digital and Analog Communication Systems	B. P. Lathi, Zhi Ding	Oxford University Press.	4th edition,
2	Communication systems	A Bruce Carlson Paul B Crilly	Mc Graw Hill	4th Edition

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://www.youtube.com/watch?v=s_vmLqT_6NQ
2	ttps://archive.nptel.ac.in/courses/117/105/117105143/
3	https://www.youtube.com/watch?v=lwt2BnOUaQY
4	https://www.youtube.com/watch?v=hTAlcrqjNps

SEMESTER S5

RENEWABLE ENERGY SYSTEMS

Course Code	**PEEVT 522**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Understand the environmental issues with conventional fuels, the new methodologies/technologies for the effective utilization of renewable energy sources.
2. Familiarize with the characteristics of solar PV and wind power sources
3. Understanding of electronic conversion systems application to renewable energy generation systems and the synchronization with smart grid systems.
4. Equip the students to pursue further specialized areas of study such as renewable energy and green consumer electronics, industrial control systems and smart grid, and renewable energy system.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Renewable Energy (RE)Sources: World energy scenario, Over view of conventional energy sources, their limitation, need of renewable energy, potential & development of renewable energy sources ,Renewable energy in India, An overview of types of renewable energy systems - Wind power, Hydropower (micro and mini), Solar energy, Biomass, Bio-fuel, Geothermal Heat energy, Pros and cons; Applications	9
2	Solar Energy: Introduction to photovoltaic (PV) systems - Principle of PV conversion; Commercial solar cell, Thin film PV device fabrication - LPCVD, APCVD, PECVD; Tandem Solar cell fabrication; Solar power extraction using PV-Cells, I-V Characteristics, PV-Inverters without D.C. to D.C. converters, stand alone and grid collected PV	9

	systems, Grid interfacing-with isolation, without isolation, Maximum power point tracking- Methods(MPPT), PV-Inverters with D.C. to D.C. converters-on low frequency side and high frequency side with isolation, without isolation.	
3	Wind Energy: Sources and potentials, Evaluation of Wind Intensity, Topography, General Classification of Wind Turbines-Rotor Turbines, Multiple-Blade Turbines, Drag Turbines, Lifting Turbines, System Toroidal Rotor Amplifier Platform (TARP)–Wind amplified rotor platform (WARP), Generators and speed control used in wind power energy: Fixed speed with capacitor bank, Rotor resistance control, SCIG and DFIG, Synchronous Generator- external magnetized, Synchronous Generator-permanent magnets.	9
4	Introduction to grid connectivity of RE systems, smart grid and emerging technologies, operating principles and models of smart gird components, key technologies for generation, networks, loads and their control capabilities; Evolution of electricity metering, key components of smart metering, overview of the hardware used for smart meters, smart metering protocols. Structure and main components of a distribution management system, Supervisory control and data acquisition (SCADA), distribution system modelling, new trends for smart grids, topology analysis, power flow analysis	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the need, importance and scope of various Non-Conventional sources of energy	**K2**
CO2	Outline the concepts and technologies related to renewable energy systems using Solar-PV	**K2**
CO3	Outline the concepts and technologies related to renewable energy systems using wind	**K2**
CO4	Understand the integration of smart grid with renewable energy systems and the fundamentals of Smart metering	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2						2					1
CO2	2											
CO3	2											
CO4	3		1									

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Solar Energy: Principles of Thermal Collection and Storage	Nayak J. K. and Sukhatme S. P.	Tata McGraw Hill.	2006
2	Power Electronics: Circuits, Devices and Applications	Muhannad H. R	Pearson Prentice Hall	2004
3	Smart Grid Technology and Applications	Nick Jenkins, JanakaEkanayake, [et al.]	Wiley India Ltd	2012
4	Design of Smart Power Grid Renewable Energy Systems	Ali Keyhani	Wiley-IEEE Press	2016

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Non-Conventional Energy Sources	G.D. Rai	Khanna Publishers	2017
2	Renewable Energy Technologies	Ramesh & Kumar	Narosa Publishing House	2018
3	Integration of alternative sources of energy	Felix A. Farret, M. Godoy simoes	Wiley-IEEE Press	2006
4	Wind power plants and projects developments	Joshua Earnest and T Wizelius	PHI, New Delhi	2011
5	Handbook of renewable energy technology	Ahmed F Zobba, Ramesh C Bansal	World Scientific, Singapore	2011

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/mh51mAUexK4?si=9O7PpRIU2ARBAVvV
2	https://youtu.be/5zAQot4pKgU?si=NH-k7lmY2ErQ5s73
3	https://youtu.be/bA-yMfHPazI?si=14PgB-_4stG9FdGC
4	https://youtu.be/vEFWXyOIYmU?si=q8UmAYoZOL0bW4_H

SEMESTER S5

GRAPH THEORY

Course Code	PEEVT523	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To introduce fundamental concepts in Graph Theory, properties and characterisation of graph/trees and graph theoretic algorithms, which are widely used in Mathematical modelling and has applications in all branches of Engineering.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Graphs : Introduction- Basic definition – Application of graphs – finite, infinite and bipartite graphs – Incidence and Degree – Isolated vertex, pendant vertex and Null graph. Paths and circuits – Isomorphism, sub graphs, walks, paths and circuits, connected graphs, disconnected graphs and components.	9
2	Eulerian and Hamiltonian graphs : Euler graphs, Operations on graphs, Hamiltonian paths and circuits, Travelling salesman problem. Directed graphs – types of digraphs, Digraphs and binary relation, Directed paths, Fleury's algorithm.	8
3	Trees and Graph Algorithms : Trees – properties, pendant vertex, Distance and centres in a tree - Rooted and binary trees, counting trees, spanning trees, Prim's algorithm and Kruskal's algorithm, Dijkstra's shortest path algorithm, Floyd-Warshall shortest path algorithm.	8
4	Connectivity and Planar Graphs : Vertex Connectivity, Edge Connectivity, Cut set and Cut Vertices, Fundamental circuits, Planar graphs, Kuratowski's theorem (proof not required), Different representations of planar graphs,	11

	Euler's theorem, Geometric dual. Graph Representations and Vertex Colouring : Matrix representation of graphs-Adjacency matrix, Incidence Matrix, Circuit Matrix, Path Matrix. Coloring- Chromatic number, Chromatic polynomial, Matchings, Coverings, Four color problem and Five color problem. Greedy colouring algorithm.	

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain vertices and their properties, types of paths, classification of graphs and trees & their properties. (Cognitive Knowledge Level: Understand)	**K2**
CO2	Demonstrate the fundamental theorems on Eulerian and Hamiltonian graphs.	**K2**
CO3	Illustrate the working of Prim's and Kruskal's algorithms for finding minimum cost spanning tree and Dijkstra's and Floyd-Warshall algorithms for finding shortestpaths.	**K3**
CO4	Explain planar graphs, their properties and an application for planar graphs.	**K3**
CO5	Explain the Vertex Color problem in graphs and illustrate an example application for vertex coloring	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**3**							**2**		**2**
CO2	**3**	**3**	**3**	**3**						**2**		**2**
CO3	**3**	**3**	**3**	**3**						**2**		**2**
CO4	**3**	**3**	**3**	**3**						**2**		**2**
CO5	**3**	**3**	**3**			**3**				**2**		**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Graph theory,	Narsingh Deo,	PHI	1979

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Graph Theory,	R. Diestel,	free online edition, 2016: diestel-graph-theory.com/ basic.html.	2016
2	Introduction to Graph Theory,	Douglas B. West	Prentice Hall India Ltd.,	2001
3	Introduction to Graph Theory,	Robin J. Wilson,	Longman Group Ltd	.,2010
4	Graph theory with Applications	A. Bondy and U.S.R. Murty		

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc22_ma10/preview
2	https://archive.nptel.ac.in/courses/111/106/111106102/
3	https://nptel.ac.in/courses/128106001

SEMESTER S5

CAD FOR VLSI DESIGN

Course Code	PEEVT524	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. Understand the different stages of design flow; the basic data structures and algorithms used in each stage
2. Understand data structures and algorithms used in recent CAD tools
3. Identify suitable data structures and propose new algorithms for CAD applications and develop new CAD tools

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Graph Terminology: Basic graph theory terminology, Data structures for representation of Graphs Search Algorithms: Breadth First Search, Depth First Search, Topological Sort Shortest Path Algorithms: Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path	9
2	VLSI Design Flow, VLSI Design Styles Partitioning: Levels of Partitioning, Parameters for Partitioning, Classification of Partitioning Algorithms, Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm	9
3	**Layout**: Layout Layers and Design Rules, Physical Design Optimizations Compaction: Applications of Compaction, Informal Problem Formulation, Graph Theoretical Formulation, Maximum Distance Constraints, Longest Path algorithm for DAG, Liao-Wong Algorithm. **Placement**: Optimization Objectives, Wirelength Estimation, Weighted	9

	Wirelength, Maximum Cut Size, Wire Density Placement Algorithms: Quadratic Placement	
4	**Floorplanning**: Optimization Objectives, Slicing Floorplan, Non-Slicing Floorplan. Floorplan Representations: Constraint Graph, Sequence Pair **Global Routing**: Terminology and Definitions, Optimization Goals, Representation of Routing Regions Maze Routing Algorithms: Lee's Algorithm, Detailed Routing: Horizontal and Vertical Constraint Graph. Channel Routing Algorithms: Left-Edge algorithm	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply Search Algorithms and Shortest Path Algorithms to find various graph solutions.	**K3**
CO2	Apply partitioning algorithms on graphs representing netlist.	**K3**
CO3	Apply different algorithms for layout compaction and placement	**K3**
CO4	Utilise different algorithms to solve floorplan and routing problems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	2							1		
CO2	3	3	2							1		
CO3	3	3	2							1		
CO4	3	3	2							1		
CO5												

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	"Algorithms for VLSI Design Automation",	Gerez,Sabih H.	John Wiley & Sons	2006.
2	Algorithms for VLSI Physical Design Automation	Sherwani, Naveed A	Kluwer Academic Publishers	1999
3	VLSI Physical Design: From Graph Partitioning to Timing Closure	Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng	Springer	2011

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Physical Design Automation: Theory and Practice	Sadiq M. Sait and H. Yousse	World Scientific	1999
2	Introduction to Algorithms.	Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest	The MIT Press	3rd edition, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/hk5rQs7TQ7E?feature=shared
2	https://youtu.be/O9guSe5_tG0
3	https://youtu.be/F44WOxhbtV0
4	https://youtu.be/TYy2o8Qy4TY

SEMESTER S5

NANOELECTRONICS

Course Code	PEEVT526	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To understand the challenges of scaling of devices to Nano-meter scales
2. To design novel transistor devices to reduce the short channel effects and to improve the performance
3. To understand the Nano-scale quantum transport in Nano electronic devices from atom to transistor
4. To apply quantum mechanics in materials and quantum devices

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to Nano electronics-Review of MOSFETs**- Band diagram-operation-threshold voltage- current-MOSFET parameters. **Challenges going to sub-100 nm MOSFETs**- Technological and physical limits of Nano electronic systems, characteristic lengths **Scaling and short channel effects**-Channel length, Oxide layer thickness, tunneling, power density, non-uniform dopant concentration, threshold voltage scaling, hot electron effects, sub threshold current, velocity saturation, DIBL, channel length modulation. **High-K gate dielectrics**- Effective oxide thickness, Effects of high-K gate dielectrics on MOSFET performance (Text books 1,2,3)	9
2	**Novel MOS Devices and Performance Optimization** **Silicon-on-insulator devices**--FD SOI, PD SOI	9

	Multiple gate MOSFETs--Double gate MOSFETs, FinFETs, Nanowires-Multi gate MOSFET physics-natural length and short channel effects. **Multi Gate MOSFET performance optimization**: Fins, Fin Width, Fin Height and Fin Pitch, Fin Surface Crystal Orientation, Fins on Bulk Silicon, Nano-wires. Gate Stack, Gate Patterning, Threshold Voltage and Gate Work function requirements, Poly silicon Gate, Metal Gate, Tunable Work function metal gate, Mobility and Strain Engineering, Nitride Stress Liners, Embedded SiGe and SiC Source and Drain, Local Strain from Gate Electrode, Substrate Strain, Strained Silicon on Insulator. (Text books 1,4)	
3	**Quantum Transport** **Atomistic view of electrical Resistance**-Energy level diagram- What makes electrons flow- The quantum of conductance - Potential profile- Coulomb blockade - Towards Ohm's law **Schrodinger equation**- Method of finite differences – Examples (particle in a box only) **Band structure**- 1-D examples- General result with basis- 2-D example **Sub bands**- Quantum wells, wires, dots, graphene and "carbon nanotubes" --Density of states-Minimum resistance of a wire **Ballistic to Diffusive Transport**-Landauer formula, Landauer-Buttiker formula. Ballistic and Diffusive transport – transmission. (Text books 3,5,6. Use MATLAB codes in the text book "Quantum transport atom to transistor" to illustrate the concepts)	**9**
4	**Applications of Quantum mechanics and Quantum devices** **Tunneling and applications of quantum mechanics**- solution of Schrodinger equation: Free space, Potential well, tunneling through a potential barrier. Potential energy profiles for material interfaces, Applications of tunneling. **Hetero junctions** -Modulation-doped hetero junctions- SiGe strained hetero structures- MODFET- Resonant tunnelling-Resonant tunnelling transistor **Single electron devices** –Coulomb blockade in a Nano capacitor, tunnel junctions, Double tunnel junction--Coulomb staircase, Single electron transistor. **Spintronics**-Transport of spin, GMR-TMR,applications, Spin Transistor (Text books 3,6)	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Describe the challenges of scaling of electron devices to Nano meter scales	**K2**
CO2	Design novel transistor devices to reduce the short channel effects and improve performance	**K3**
CO3	Outline the Nano scale quantum transport in Nano electronic devices from atom to transistor	**K2**
CO4	Apply quantum mechanics in materials and quantum devices	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2									3
CO2	3	3	3									3
CO3	3	3	2									3
CO4	3	3	3									3

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of Modern VLSI Devices	Yuan Taur, Tak H Ning	Cambridge University Press,	Second edition 2009
2	Nanoelectronics and Nanosystems	Karl Goser· Peter GlÖsekötter· Jan Dienstuhl	Springer-Verlag Berlin Heide1berg	First Edition, 2004
3	Nanotechnology for microelectronics and optoelectronics,	J M Martinez Duart, R J Martin Palma, F Agullo Rueda	Elsevier,	First Edition, 2006
4	FinFETs and Other multigate Transistors	J-P Colinge	Springer	First Edition, 2008
5	Quantum Transport Atom to Transistor	Supriyo Datta	Cambridge University Press	First Edition, 2005
6	Fundamentals of nano electronics,	George W.Hanson,	Pearson Education.	First Edition 2009

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of Carrier Transport	Mark Lundstrom	Cambridge University Press	Second Edition, 2000
2	High Dielectric Constant materials VLSI MOSFET Applications,	H R Huff, D C Gilmer,	Springer	First Edition, 2004
3	Nanoelectronics and nanosystems From Transistors to Molecular and Quantum Devices	Karl Goser· Peter GlÖsekötter· Jan Dienstuhl	Springer	First Edition, 2004
4	NANOSCALE TRANSISTORS Device Physics, Modeling and Simulation	Mark S. Lundstrom, Jing Guo	Springer	First Edition, 2006
5	Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs	Jerry G. Fossum, Vishal P. Trivedi	Cambridge University Press	First Edition, 2013
6	Introduction to Nanotechnology	Charles P Poole jr. Frank J Owens	John Wiley and Sons	First Edition, 2003
7	Introduction to Quantum Mechanics	David J Griffiths, Darrel F schroetter	Cambridge University Press	Third Edition, 2018

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117108047, https://nanohub.org/resources/5328
2	https://nptel.ac.in/courses/117108047
3	https://nptel.ac.in/courses/117107149, https://nanohub.org/resources/8086,, https://nanohub.org/courses/FON1, https://nanohub.org/resources/5306
4	https://nptel.ac.in/courses/117107149, https://nanohub.org/resources/8086

SEMESTER S5

REAL TIME OPERATING SYSTEMS

Course Code	PEEVT 527	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBEVT504, PBECT404 (Course code)	Course Type	Theory

Course Objectives:

1. To develop skills in Real Time operating system to apply the same in real life applications.
2. Understand the concept of real time operating system along with its synchronization, communication and interrupt handling tools.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Operating system: Types, Objectives and functions, Kernel, Process - States, Process Control Block, Operations on processes.	9
2	Process Scheduling: FCFS, SJF, Priority, Round-Robin, Multilevel Queue and Multilevel Feedback Queue Scheduling. Thread: Structure. User and Kernel level threads, multi-threading models, multiprocessor scheduling.	9
3	Real Time Operating Systems: Structure and characteristics of Real Time Systems, Task: Task states, Task synchronization -Semaphores- types, Inter Task communication mechanisms: message queues, pipes, event registers, signals, Exceptions and interrupt handling.	9
4	Task constraints, Task scheduling: Aperiodic task scheduling: EDD. EDF, LDF, EDF with precedence constraints. Periodic task scheduling: Rate monotonic and Deadline monotonic, Real time Kernel- Structure, State transition diagram, Kernel primitives. Features of Free RTOS and Linux, Case study of (Kernel design, threads and task scheduling) RTOS: MicroC/OS-II, RTOS control system used in real life applications - in adaptive cruise Control	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Summarize the functions and structure of general-purpose operating systems.	**K2**
CO2	Use different scheduling algorithms on processes and threads.	**K3**
CO3	Interpret a real time operating system along with its synchronization, communication and interrupt handling tools.	**K2**
CO4	Illustrate task constraints and analyse the different scheduling algorithms on tasks.	**K4**
CO5	Illustrate the applications of real time operating systems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	3		1							2
CO2	2	3	2								2	2
CO3	3	3	2		2						3	2
CO4	3	2	3								2	2
CO5	3	3	2		1						2	3

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Operating System Principles	Abraham Silberschatz	Wiley India	7th edition, 2011
2	Operating systems- Internals and design principles	William Stallings	Prentice Hall	7th edition, 2011
3	Real-Time Concepts for Embedded Systems	Qing Li	CMP Books	2nd Edition,2013
4	HARD REAL-TIME COMPUTING SYSTEMS Predictable Scheduling Algorithms and Applications	Giorgio C. Buttazzo	Kluwer Academic Publishers	1st Edition,1997

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Modern Operating Systems	Tanenbaum	Pearson Edition	3rd Edition, 2007
2	Micro C/OS-II, The Real Time Kernel	Jean J Lambrosse	CMP Books	2nd Edition,2011
3	Real-Time Systems: Theory and Practice	Rajib Mall	Pearson	1st Edition,2008
4	An Embedded Software Primer	David E Simon	Pearson	2nd Edition,2012

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/106/105/106105172/ - Week 1
2	https://archive.nptel.ac.in/courses/106/105/106105172/ - Week 2
3	https://archive.nptel.ac.in/courses/106/105/106105172/ - Week 3
4	https://archive.nptel.ac.in/courses/106/105/106105172/ - Week 4

SEMESTER S5

CAD BASED VLSI DESIGN OPTIMIZATION

Course Code	PEEVT525	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	5/3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	5 Credit Elective

Course Objectives:

1. Understand the different stages of design flow; the basic data structures and algorithms used in each stage
2. Understand data structures and algorithms used in recent CAD tools
3. Identify suitable data structures and propose new algorithms for CAD applications and develop new CAD tools

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Graph Terminology: Basic graph theory terminology, Data structures for representation of Graphs Search Algorithms: Breadth First Search, Depth First Search, Topological Sort Shortest Path Algorithms: Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path	9
2	The VLSI Design Problem, The Design Domains, A Quick Tour of VLSI Design Automation Tools: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods VLSI Design Flow, VLSI Design Styles Partitioning: Levels of Partitioning, Parameters for Partitioning, Classification of Partitioning Algorithms, Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm	9
3	**Layout**: Layout Layers and Design Rules, Physical Design Optimizations	9

	Compaction: Applications of Compaction, Informal Problem Formulation, Graph Theoretical Formulation, Maximum Distance Constraints, Longest Path algorithm for DAG, Liao-Wong Algorithm, The Bellman-Ford Algorithm **Placement**: Optimization Objectives, Wirelength Estimation, Weighted Wirelength, Maximum Cut Size, Wire Density Placement Algorithms: Constructive Placement, Iterative Improvement Partitioning: The Kernighan-Lin Partitioning Algorithm	
4	**Floorplanning**: Optimization Objectives, Slicing Floorplan, Non-Slicing Floorplan. Floorplan Representations: Constraint Graph, Sequence Pair **Global Routing**: Terminology and Definitions, Optimization Goals, Representation of Routing Regions Maze Routing Algorithms: Lee's Algorithm, Detailed Routing: Horizontal and Vertical Constraint Graph. Channel Routing Algorithms: Left-Edge algorithm General Remarks on VLSI Simulation.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Internal Ex	Evaluate	Analyse	Total
5	**15**	**10**	**10**	**40**

Criteria for Evaluation (Evaluate and Analyse): 20 marks

1. Literature Review and Report (10 Marks)

Assessment Method:

- Students review recent publications on a specific topic related to VLSI design (e.g., advancements in layout optimization or new algorithms for partitioning).
- Preparation of a detailed report summarizing the findings, discussing the significance, and suggesting potential improvements or future research directions.

Criteria:

- Relevance of Chosen Publications (2 Marks): Selection of up-to-date and relevant research papers.

- Depth of Analysis (4 Marks): Thorough understanding and critical analysis of the literature.
- Clarity and Organization (2 Marks): Well-structured and clearly written report.
- Originality (2 Marks): Innovative insights or perspectives on the topic.

2. VLSI Design Flow Understanding and Report (5 Marks)

Assessment Method:

- Students study the VLSI design flow, including partitioning, placement, and floor planning.
- Preparation of a comprehensive report explaining each step of the design flow, the tools used, and their features.

Criteria:

- Comprehensiveness (2 Marks): Detailed explanation of each step in the VLSI design flow.
- Tool Proficiency (1 Mark): Understanding of the various EDA tools used in the design process.
- Clarity and Detail (1 Mark): Clear and detailed presentation of information.
- Analytical Skills (1 Mark): Critical analysis of the design flow and tool features.

3. Graph Theory and Algorithms Practical Assignment (5 Marks)

Assessment Method:

- Students implement and test various graph algorithms (e.g., Dijkstra's algorithm, Floyd-Warshall algorithm) using appropriate data structures.
- Submit a report with their implementation, test cases, and performance analysis.

Criteria:

- Correctness of Implementation (2 Marks): Accurate implementation of graph algorithms.
- Performance Analysis (1 Mark): Detailed analysis of the algorithm performance on different test cases.
- Clarity and Presentation (1 Mark): Well-organized and clearly written report.
- Problem-Solving Skills (1 Mark): Ability to troubleshoot and optimize the implementation.

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. Each question carries 9 marks. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply Search Algorithms and Shortest Path Algorithms to find various graph solutions.	**K3**
CO2	Apply partitioning algorithms on graphs representing netlist.	**K3**
CO3	Apply different algorithms for layout compaction and placement	**K3**
CO4	Utilise different algorithms to solve floorplan and routing problems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2							1		
CO2	3	3	2							1		
CO3	3	3	2							1		
CO4	3	3	2							1		

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	"Algorithms for VLSI Design Automation",	Gerez,Sabih H.	John Wiley & Sons	2006.
2	Algorithms for VLSI Physical Design Automation	Sherwani, Naveed A	Kluwer Academic Publishers	1999
3	VLSI Physical Design: From Graph Partitioning to Timing Closure	Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng	Springer	2011

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Physical Design Automation: Theory and Practice	Sadiq M. Sait and H. Yousse	World Scientific	1999
2	Introduction to Algorithms.	Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest	The MIT Press	3rd edition, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/hk5rQs7TQ7E?feature=shared
2	https://youtu.be/O9guSe5_tG0
3	https://youtu.be/F44WOxhbtV0
4	https://youtu.be/TYy2o8Qy4TY

SEMESTER: S5

DIGITAL IC DESIGN LAB

Course Code	PCEVL507	CIE Marks	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	ESE Marks	50
Credits	2	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304 Logic Circuit Design PCEVT402 Digital System Design	Course Type	Lab

Course Objectives:

1. Develop a fundamental understanding of digital logic gates and their implementation using Verilog.
2. Learn the principles of designing and implementing basic combinational and sequential circuits.
3. Develop the ability to synthesize complex digital circuits using EDA tools such as FOSS tools, Cadence, and Synopsys.
4. Gain experience in using synthesis tools to optimize and implement digital circuits

Details of Experiment

Expt. No	Experiment
1	Write Verilog codes to realize the logic gates: AND, OR, NOT, XOR and XNOR
2	Write Verilog codes to realize a 2-bit half adder in all three modeling styles
3	Write a structural Verilog code to realize a 2-bit full adder
4	Write a Verilog code to realize a 2-bit full adder using two half adders
5	Write a behavioural Verilog code to realize a 8:1 MUX
6	Write a behavioural Verilog code to realize a 1:16 DE-MUX
7	Write a behavioural Verilog code to realize a 16:4 encoder
8	Write a behavioural Verilog code to realize a 3:8 decoder
9	Write Verilog codes to realize SR, D, JK and T flip-flops
10	Realize a 3-bit comparator in Verilog using behavioural and structural modeling

11	Realize ring and Johnson counters in Verilog using data-flow modeling
12	Realize a BCD counter in Verilog using gate level abstraction (structural modeling)
13	Synthesize the basic logic gates using FOSS/Cadence/Synopsys tool
14	Synthesize both half adder and full adder using FOSS/Cadence/Synopsys tool
15	Realize a FIFO in Verilog and synthesize using FOSS/Cadence/Synopsys tool

Course Assessment Method (CIE: 50 Marks, ESE 50 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work, experiments, Viva and Timely completion of Lab Reports / Record. (Continuous Assessment)	Internal Exam	Total
5	25	20	50

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

Mandatory requirements for ESE:

- Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.
- Endorsement by External Examiner: The external examiner shall endorse the record.

Course Outcomes (COs)

At the end of the course the student will be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Demonstrate the ability to write Verilog code to implement fundamental logic gates and verify the functionality of implemented logic gates through simulation and testbenches.	**K2**
CO2	Get familiarity in various modeling styles (behavioral, dataflow, and structural) to realize combinational and sequential circuits.	**K2**
CO3	Demonstrate the ability to synthesize Verilog code for complex digital circuits using EDA tools such as FOSS, Cadence, and Synopsys.	**K3**
CO4	Ability to use synthesis tools to optimize digital circuits for performance, area, and power.	**K4**
CO5	Ability to produce and present detailed reports on the synthesis and optimization process	**K5**

K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3			2							
CO2	2	3			2							
CO3	3	3	3		3							
CO4	2	3	3	3	3							

1: Slight (Low),2: Moderate (Medium),3: Substantial (High), : No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL Synthesis: A Practical Primer	J. Bhasker	B. S. Publications,	2001
2	Fundamentals of Logic Design	Roth C.H	Jaico Publishers. V Ed., 2009	5th Edition
3	Digital Principles & Design	Donald G Givone	McGraw Hill Education	2017
4	Digital Design: Principles and Practices	John F Wakerly	Pearson India	4th, 2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL : A guide to digital design and synthesis	Palnitkar S.,	Prentice Hall; 2003.	2nd Edn.,
2	ASIC Design and Synthesis RTL Design Using Verilog	Vaibbhav Taraate	Springer	2021
3	FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version	Pong P. Chu	Wiley	2008

Video Links (NPTEL, SWAYAM…)	
Sl. No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/
2	https://archive.nptel.ac.in/courses/117/106/117106086/

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. Lab Reports and Record Keeping (6 Marks)

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. Viva Voce (5 Marks)

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. Procedure/Preliminary Work/Design/Algorithm (10 Marks)

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.

- Creativity and logic in algorithm or experimental design.

2. Conduct of Experiment/Execution of Work/Programming (15 Marks)

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. Result with Valid Inference/Quality of Output (10 Marks)

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. Viva Voce (10 Marks)

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. Record (5 Marks)

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER S5

FPGA LABORATORY

Course Code	**PCEVL508**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304 Logic Circuit Design PCEVT402 Digital System Design	**Course Type**	Lab

Course Objectives:

1. Equip students with the skills to write, test, and debug VHDL code for various digital circuits.
2. Enable students to design and implement basic digital components such as logic gates, multiplexers, adders, counters, and registers on FPGA.
3. Enable students to design and implement sequential circuits, including various types of flip-flops, sequence detectors, and counters, on FPGA.
4. Guide students in designing, implementing, and optimizing complex digital systems, such as ALUs and FIFO buffers, on FPGA.

Details of Experiment

Expt. No	Experiment
1	Realize basic the logic gates in VHDL and implement on FPGA
2	Realize a 4:1 MUX in VHDL and implement on FPGA
3	Realize a 1:8 DEMUX in VHDL and implement on FPGA
4	Realize a half adder in VHDL and implement on FPGA
5	Realize a full adder in VHDL and implement on FPGA
6	Realize a 2-bit comparator in VHDL and implement on FPGA
7	Realize a 4-bit shift register in VHDL and implement on FPGA
8	Realize a FIFO in VHDL and implement on FPGA
9	Realize a 4-bit adder in VHDL and implement on FPGA
10	Realize a Up/Down counter in VHDL and implement on FPGA
11	Realize a Mealy and Moore sequence detector to detect the sequence 1010 in VHDL and

	implement on FPGA
12	Realize an asynchronous BCD counter in VHDL and implement on FPGA
13	Realize a 4-bit Gray to Binary in VHDL and implement on FPGA
14	Realize the flipflops D, JK and T in VHDL and implement on FPGA
15	Realize in VHDL a 4-bit ALU that performs basic arithmetic (addition, subtraction) and logic (and, or, xor) operations on 4-bit inputs and implement on FPGA . Understand the synthesis reports and perform timing and power analysis.

Course Assessment Method (CIE: 50 Marks, ESE 50 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work, experiments, Viva and Timely completion of Lab Reports / Record. (Continuous Assessment)	Internal Exam	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	**15**	**10**	**10**	**5**	**50**

Mandatory requirements for ESE:

- Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.
- Endorsement by External Examiner: The external examiner shall endorse the record.

Course Outcomes (COs)

At the end of the course the student will be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Write, test, and debug VHDL code to accurately describe and implement a variety of digital circuits.	**K2**
CO2	Design and implement fundamental digital components, such as logic gates, multiplexers, adders, and counters, using FPGA technology.	**K3**
CO3	Design, implement, and analyze sequential circuits, including flip-flops, sequence detectors, and various types of counters, on FPGA.	**K3**
CO4	Integrate multiple digital components into complex systems, such as ALUs and FIFO buffers, and optimize these systems for performance and resource efficiency on FPGA.	**K4**

K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3			2				1			
CO2	2	3			2				1			
CO3	3	3	3		3				1			
CO4	2	3	3	3	3				2			

1: Slight (Low),2: Moderate (Medium),3: Substantial (High), : No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Design with RTL Design, VHDL, and Verilog	Frank Vahid	Wiley	2010
2	VHDL for Engineers	Kenneth L. Short	Pearson	1st Edition, 2008
3	FPGA Prototyping by VHDL Examples: Xilinx MicroBlaze MCS SoC	Pong P. Chu	Wiley	2018
4	Digital Systems Design Using VHDL	Charles H. Roth Jr., Lizy Kurian John	Cengage Learning	2007

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VHDL: Programming by Example	Douglas L. Perry	McGraw-Hill	4th Edition, 2002
2	Circuit Design with VHDL	Volnei A. Pedroni	MIT Press	2nd Edition, 2010
3	The Designer's Guide to VHDL	Peter J. Ashenden	Morgan Kaufmann	3rd Edition, 2008

Video Links (NPTEL, SWAYAM…)	
Sl. No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/108/117108040/
2	https://nptel.ac.in/courses/108106177

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. Lab Reports and Record Keeping (6 Marks)

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. Viva Voce (5 Marks)

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. Procedure/Preliminary Work/Design/Algorithm (10 Marks)

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.

- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
- Creativity and logic in algorithm or experimental design.

2. Conduct of Experiment/Execution of Work/Programming (15 Marks)

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. Result with Valid Inference/Quality of Output (10 Marks)

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. Viva Voce (10 Marks)

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. Record (5 Marks)

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER 6

Electronics Engineering (VLSI Design and Technology)

SEMESTER 6

ANALOG VLSI DESIGN

Course Code	PCEVT601	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-1-0-0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs.30 Min.
Prerequisites (if any)	PCECT302,PCECT303	Course Type	Theory

Course Objectives:

1. A foundation in the fundamentals of Analog VLSI Design
2. Ability to Design of IC MOS Amplifiers and PLL
3. An Introduction to challenges facing in Analog IC Design

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**2-Terminal MOS Structure** - Flat Band Voltage, Potential Balance and Charge, Effect of Gate-Body Voltage on Surface Condition General Analysis. Inversion: Strong and Weak Inversion, Small Signal Capacitance.	11
2	**3-Terminal MOS Structure** - Contacting Inversion Layer, General Analysis, Body-effect, Pinch-off voltage. Introduction, Regions of Operation.	11
3	**4-Terminal MOS Structure** – Introduction, Complete All-Region Model – Current Equations, Simplified All-Region Models: Linearizing Depletion Region Charge, Source-Referenced Simplified All- Region Models. Strong Inversion: Complete Strong Inversion Model- Non Saturation	11
4	**Single-Stage Amplifiers** - Introduction to basic amplifier Configurations: Gate-Drain Connected Loads: CS, Frequency Response, Noise Analysis, Current-Source Load: CS (only CS) Cascode, Push-pull amplifier **Noise**:Types of Noise: Thermal, Flicker, Shot Noise.	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Gives students structural idea about 2 terminal MOSFET.	**K2**
CO2	Gives students structural idea about 3 terminal MOSFET	**K2**
CO3	This module gives students structural idea about 4 terminal MOSFET and strong inversion models.	**K1**
CO4	This module deals about Single stage amplifiers and its active loads and different types of Noises.	**K1**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	1									
CO2	3	3	-									
CO3	2	2	-									
CO4	3	2	1									

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Operation and Modeling of the MOS Transistor	YannisTsividis Colin McAndrew	3/e, 2010	OUP
2	CMOS – Circuit Design, Layout, andSimulation	R. Jacob Baker, Harry W Li,David E Boyce	1998.	3rd Edition, .
3	Design of Analog CMOS Integrated Circuits	BehzadRazavi	2008	Tata McGraw Hill
4	CMOS Analog Circuit Design	Philip E Allen, Douglas R Holberg	2010	International Student(Second) Edition, First Indian Edition
5	CMOS – Circuit Design, Layout, andSimulation	R. Jacob Baker, Harry W Li,David E Boyce	1998.	3rd Edition, .

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS, CIRCUIT Design, Layout and Simulation	Baker, Harry, David	3/e	PHI

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117101105
2	https://nptel.ac.in/courses/117101105
3	https://nptel.ac.in/courses/117101105
4	https://nptel.ac.in/courses/117101105

SEMESTER S6

SYSTEM ON CHIP DESIGN

Course Code	PCEVT602	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs.30 Min.
Prerequisites (if any)	PCEVT501 Digital CMOS Design	Course Type	Theory

Course Objectives:

1. Understand the SoC design process, including the differences between waterfall and spiral models, and the significance of top-down versus bottom-up approaches in meeting specification requirements.
2. Develop the ability to create a comprehensive design specification and execute top-level macro design, utilizing appropriate tools and methodologies for macro integration and productization.
3. Apply best practices in RTL coding, with a focus on proper clock and reset handling to ensure reliable and efficient design implementation.
4. Master the design and integration of hard macros, addressing key issues such as design for testability, power distribution, and model development, to produce robust and deliverable macro products.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	System On Chip Design Process: A canonical SoC Design, SoC Design flow - Waterfall vs spiral, Top-down vs Bottom up, Specification requirement, Types of specification, System design process, System level design issues- Soft IP vs Hard IP.	9
2	Macro Design Process: Contents of a design specification, Top level Macro Design,Top level Macro Design Process, Activities and tools, Subblock design, Macro integration, Soft macro productization.	9
3	RTL coding guidelines: Overview of coding guidelines, Guidelines for	9

	clocks and resets - Mixed clock edges, Clock buffers, Gated clocks, Internally generated clocks, Gated clocks, Internally generated resets.	
4	Developing hard macros: Design issues for hard macros – Design for test, Clock and reset, Aspect ratio, Porosity, Pin placement, Power distribution. The hard macro design process, Block integration for hard macros, Productization for hard macros, Model development for hard macros, Soft macro deliverables, Hard macro deliverables.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the SoC design flow, differentiate between design methodologies, and address system-level design issues.	**K2**
CO2	Develop and implement design specifications for macro design, including integration and productization of soft macros.	**K3**
CO3	Demonstrate proficiency in applying RTL coding guidelines, effectively managing clocks and resets in their designs.	**K3**
CO4	Design, integrate, and productize hard macros, with an understanding of design issues and deliverables specific to hard macro development	**K4**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**1**	**1**	**1**				**1**			
CO2	**3**	**3**	**2**	**1**	**1**				**1**			
CO3	**3**	**3**	**2**	**1**	**2**				**1**			
CO4	**3**	**3**	**2**	**2**	**2**				**1**	**1**		**1**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Reuse Methodology manual for System-On-A-Chip Designs	Michael Keating, Pierre Bricaud	Springer	2002
2	System-on-Chip Design with Arm® Cortex® -M Processors	JOSEPH YIU	arm Education Media	2019
3	Digital VLSI Chip Design with Cadence and Synopsys CAD Tools	Erik Brunvand	Pearson	1st, July 2009
4	SoC Verification-Methodology and Techniques,	Prakash Rashinkar, Peter Paterson and Leena Singh,	Kluwer Academic Publishers,	2001

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital systems Testing and testable Design	Miron Abramovici, Melvin A. Breur, Arthur D. Friedman	Jaico Publishing House,	2001
2	Hardware Design Verification: Simulation and Formal Method-based Approaches	William K.Lam	Prentice Hall Professional Technical Reference	2005
3	Design of System on a ChipDevices & Components	Ricardo Reis, Jochen A. G. Jess	Springer	2004

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/108106191
2	https://nptel.ac.in/courses/108106177
3	https://nptel.ac.in/courses/106105161
4	https://www.arm.com/why-arm/custom-socs
5	https://www.youtube.com/watch?v=dokgLSAhqHI

SEMESTER S6

CONTROL SYSTEMS

Course Code	**PEEVT 631**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs.30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Teach mathematical modelling and calculate the transfer function of a system.
2. Discuss the time domain response of first and second order systems.
3. Demonstrate the steps to find the absolute stability of a system.
4. Demonstrate the steps frequency analysis of systems.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction:** Basic Components of a Control System, Open-Loop Control Systems and Closed-Loop Control Systems, Examples of control system. **Mathematical modelling of control systems:** Electrical Systems and Mechanical systems. **Transfer Function from Block Diagrams and Signal Flow Graphs:** impulse response and its relation with transfer function of linear systems. Block diagram representation and reduction methods, Signal flow graph and Mason's gain formula.	**9**
2	**Time Domain Analysis of Control Systems:** Introduction- Standard Test signals, Time response specifications. Time response of first and second order systems to unit step input and ramp inputs, time domain specifications. **Steady state error and static error coefficients.** **Frequency domain analysis:** Frequency domain specifications, correlation between time and frequency responses.	**9**

3	**Stability of linear control systems:** Concept of BIBO stability, absolute stability, Routh Hurwitz Criterion, Effect of P, PI & PID controllers. **Root Locus Techniques:** Introduction, properties and its construction, Application to system stability studies. Illustration of the effect of addition of a zero and a pole.	**9**
4	**Nyquist stability criterion:** Fundamentals and analysis. **Relative stability:** gain margin and phase margin. Stability analysis with Bode plot. **Design of Compensators:** Need of compensators, design of lag and lead compensators using Bode plots.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
● 2 Questions from each module. ● Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	● Each question carries 9 marks. ● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Determine transfer function of electromechanical systems using block diagram reduction and SFG.	**APPLY**
CO2	Determine Transient and Steady State behaviour of systems using standard test signals.	**APPLY**
CO3	Determine absolute stability and relative stability of a system using Routh Hurwitz Criterion and Root Locus Techniques.	**APPLY**
CO4	Design a control system with suitable compensation techniques using frequency domain techniques.	**APPLY**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	-	-	-	-	-	-	-	-	-	1
CO2	2	3	-	-	-	-	-	-	-	-	-	1
CO3	2	3	-	-	-	-	-	-	-	-	-	1
CO4	2	3	-	-	-	-	-	-	-	-	-	1
CO5	2	3	-	-	-	-	-	-	-	-	-	1

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Automatic Control Systems	Farid Golnaraghi, Benjamin C. Kuo	Wiley India	9th Edition, 2009
2	Control Systems Engineering	I.J. Nagarath, M.Gopal	New Age International Pub. Co.	5th Edition, 2007
3	Schaum's Outline of Feedback and Control Systems	Joseph J. DiStefano, Allen Stubberud, Ivan J. Williams	Mc Graw Hill	3rd Edition, 2013

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Control System Engineering	Norman S. Nise	Wiley India.	5th Edition and 2009
2	Modern Control Engineering	Ogata K.,	Prentice Hall of India, Pearson Education	4th Edition and 2002

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/RcuGxWc0HyQ https://youtu.be/PLgxjVQ6sZ8 https://youtu.be/fsxSst10_cE https://youtu.be/E56sENH6hLU https://youtu.be/2hK8RGVWwJs
2	https://youtu.be/8-J0Y7bvVz0 https://youtu.be/z2IpQaGHNlU https://youtu.be/LQ46V5OzEws https://youtu.be/8WYLEsa6dlY
3	https://youtu.be/UTQOQzIYKu0 https://youtu.be/3IM57uKQnXc https://youtu.be/86uzST3SM-0 https://youtu.be/wRnz0JgMIsY
4	https://youtu.be/gueIWqhJDn8 https://youtu.be/JbuTgcb7Tys https://youtu.be/g-ptzF3w94Y https://youtu.be/VCQVsolxCCE https://youtu.be/VSDLCdKfzMo https://youtu.be/w741WYd4Fe4 https://youtu.be/zkdhvPbqJLM https://youtu.be/JCBsyUp3CPw https://youtu.be/_3e6xFyFmAQ https://youtu.be/8zpb1nb082g

SEMESTER S6

VLSI VERIFICATION

Course Code	PEEVT 632	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304	Course Type	Theory

Course Objectives:

This Course aims to impart the knowledge of

1. The fault modelling and fault detection.
2. The concepts of test generation for combinational circuits
3. The concepts of test generation methods – DFT, BIST.
4. concepts of fault diagnosis

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction, VLSI design flow, need of Pre-silicon verification and post-silicon validation and debug -Role of Testing -Yield-ATE. Fault Modelling - single stuck-at-faults, Bridging faults, delay faults -functional equivalence and fault collapsing, Dominance collapsing and check point theorem. Logic and Fault Simulation - serial and parallel fault simulation.	9
2	Testability Measures- Combinational Controllability - Combinational Observability. Combinational ATPG-Path sensitization method , Boolean Difference Method-D-Algorithm-PODEM	9
3	Design for Testability – DFT Fundamentals, Scan design, Partial Scan, Random Access Scan	9
4	BIST- LFSR Pattern Generation-Output Response Analysis-BILBO. Boundary Scan standard. Introduction to Formal Design Verification. Introduction to Fault Diagnosis and Self-checking design.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Apply Fault equivalence and Fault collapsing	**KL3**
CO2	Apply basic ATPG Algorithms used in VLSI Testing.	**KL3**
CO3	Explain the concept of DFT	**KL2**
CO4	Apply BIST for output response analysis	**KL3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**										**2**
CO2	**3**	**3**										**2**
CO3	**3**	**3**										**2**
CO4	**3**	**3**										**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits	Viswani D Agarwal and Michael L Bushnell	Kluwer Academic Publishers	2000

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	High-Level Synthesis: Introduction to Chip and System Design	D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin	Springer	1st edition, 1992.
2	Digital systems Testing and Testable Design	M. Abramovici, M A Breuer and A D Friedman	IEEE Press	1994
3	Testing of Digital Systems	Niraj Jha and Sanjeep K Gupta	Cambridge University Press	2003
4	Digital Circuit Testing and Testability	P.K. Lala	Academic Press	2002

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/kW70cVmWSR8?si=B0u137fAG1Nrzu7X
2	https://youtu.be/zekvZgaK54o?si=wU-Uiu8LucspC7W4
3	https://youtu.be/FBjTy-JMZ8Y?si=7tU4qs353srSPjsg
4	https://youtu.be/5jBAVSN_U0g?si=tGa7U4OjiiojAYfw

SEMESTER S6

EMBEDDED LINUX SYSTEMS

Course Code	**PEEVT 633**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PBEVT504 Embedded System Design	**Course Type**	Elective

Course Objectives:

1. Understand the fundamental concepts of Embedded Linux, including its advantages, system architecture, development setups, and supported processor architectures.
2. Gain proficiency in setting up and using the GNU toolchain for cross-platform development, including configuring and using various development tools and IDEs.
3. Learn to select, configure, compile, and install the Linux kernel, along with understanding the structure and components of the root file system and storage device manipulation.
4. Develop the ability to set up various types of filesystems for embedded devices, configure bootloaders, and gain an introduction to device drivers.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction: Embedded Linux, Real Time Linux, Types of Embedded Linux systems, Advantages of Linux OS, Using distributions, Examples of Embedded Linux systems - system architecture, Types of host/target architectures for the development of Embedded Linux Systems, Debug setups, Boot Configurations, Processor architectures supported by Linux.	**9**
2	Cross platform Development toolchain: GNU tool chain basics, Kernel Headers Setup, Binutils setup, Bootstrap Compiler Setup, Library Setup, Full Compiler Setup, Using the tool chain. C library alternatives, JAVA, Perl, Python, Ada, IDEs , Terminal Emulators.	**9**

3	Kernel and Root File System, Kernel Considerations- selection, configuration, Compiling and Installing the kernel Root File System Structure, Libraries, Kernel Modules, Kernel Images, Device Files, Main System Applications, Custom Applications, System Initialization. Storage Device Manipulation. MTD Supported Devices, Disk Devices, Swapping.	**9**
4	Root Filesystem Setup : Filesystem Types for Embedded Devices, Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem, Placing a Disk Filesystem on a RAM Disk, Rootfs and Initramfs, Setting Up the Bootloader, Embedded Bootloaders, Introduction to Device Drivers.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain the components, advantages, and architectures of Embedded Linux systems, as well as the development and debugging setups used.	**K2**
CO2	Gain proficiency in setting up and using the GNU toolchain and other development tools for cross-platform development, including various programming languages and IDEs.	**K3**
CO3	Demonstrate the ability to select, configure, compile, and install the Linux kernel, and understand the root file system structure and storage device manipulation.	**K3**
CO4	Gain the capability to set up different types of filesystems for embedded devices, configure bootloaders, and understand the basics of device drivers	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**	**1**	**1**	**1**	**1**				**1**	**1**		
CO2	**2**	**2**	**2**	**1**	**3**				**1**	**1**		
CO3	**2**	**2**	**3**	**2**	**3**				**2**	**2**		
CO4	**2**	**2**	**3**	**2**	**3**				**2**	**2**		

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Building Embedded Linux Systems	Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, and Philippe Gerum	O'Reilly Media, Inc.	**2nd , 2008**
2	Linux Device Drivers	Alessandro Rubini, Jonathan Corbet	O'Reilly Media, Inc.	**3rd, 2005**
3	Embedded Linux Primer A Practical Real – World Approach	Christopher Hallinan	Prentice Hall	**1st 2006**

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Embedded Linux System Design and Development	P Raghavan, Amol Lad, Sriram Neelakandan	CRC Press	2005
2	Essential Linux Device Drivers	Alan Cox, Sreekrishnan, Venkateswaran	Prentice Hall	1st, 2008
3	Embedded Linux - Hardware, Software and Interfacing	Craig Hollabaugh	Pearson Education	2002

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/106105193
2	https://nptel.ac.in/courses/117106113
3	https://elearn.nptel.ac.in/shop/partnering-courses/embedded-linux-batch-3/?v=c86ee0d9d7ed
4	https://www.youtube.com/watch?v=Sk9TatW9ino

SEMESTER S6

SPEECH AND AUDIO PROCESSING

Course Code	PEEVT 634	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To impart the basic concepts of speech signal processing
2. To familiarize the auditory mechanism and speech perception

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Speech Production: - Acoustic theory of speech production- -Source/Filter model - Pitch, Formant, Spectrogram-- Discrete model for speech production, Articulatory Phonetics -Acoustic Phonetics- Basic speech units and their classification.	9
2	Short-Time Speech Analysis, Windowing, STFT, spectra of windows- Wide and narrow band spectrogram -Time domain parameters (Short time energy, short time zero crossing Rate, ACF). Frequency domain parameters-Filter bank analysis. STFT Analysis. Prosody of speech. MFCC-computation, LPC Model, Pitch and Formant Estimation.	9
3	Speech Enhancement: Spectral subtraction and Filtering, Harmonic filtering, parametric resynthesis. Speaker Recognition: Speaker verification and speaker identification- log-likelihood. Machine learning models in Speaker Recognition. Language identification: implicit and explicit models.	9
4	Signal Processing models of audio perception: Basic anatomy of hearing System: Basilar membrane behaviour. Sound perception: Auditory Filter Banks, Critical Band Structure, Absolute Threshold of Hearing, Masking-	9

	Simultaneous Masking, Temporal Masking. Models of speech perception	

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	To describe the fundamental concepts, principles, and theories of speech production	**K1**
CO2	To analyse the speech signal in the time and frequency domain	**K2**
CO3	To apply speech processing concepts in real-world applications	**K3**
CO4	To describe the fundamental concepts, principles, and theories of hearing mechanism	**K1**
CO5	To develop applications by combining concepts of speech production and hearing mechanism	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3											
CO2	3	2										
CO3	3	2										
CO4	3											
CO5	3	2	3	3	3	3		2				

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Speech Communications: Human and Machine, 2nd Edition	Douglas O'Shaughnessy	Wiley-IEEE Press	2nd edition
2	Discrete-Time Speech Signal Processing: Principles and Practice	Thomas F. Quatieri	Prentice-Hall Signal Processing Series	2001

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Processing of Speech Signals	Rabinar	Pearson	2003

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	Speech and Audio Processing 1: Introduction to Speech Processing - Professor E. Ambikairajah https://www.youtube.com/watch?v=Xjzm7S__kBU
2	Speech Analysis - Professor E. Ambikairajah https://www.youtube.com/watch?v=Y_mSQ7tTlvQ&t=38s
3	Speech and Audio Processing 1: Introduction to Speech Processing - Professor E. Ambikairajah https://www.youtube.com/watch?v=Xjzm7S__kBU
4	Video Links available on hearing anatomy

SEMESTER S6

SEMICONDUCTOR DEVICE MODELING

Course Code	**PEEVT 636**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Solid State Devices (PCECT302)	**Course Type**	Elective

Course Objectives:

1. This course explains the qualitative understanding of the physics of the semiconductor devices and conversion of this understanding into equations
2. To introduce students to the field of compact modeling and familiarize them with the methods for the model development

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Semiconductor device modeling overview:** Types of device models- Numerical Models, Analytical models, compact models. **PN Junction diode:** DC Current-Voltage Characteristics, Limitations of the ideal diode model, Static model of the ideal diode and its implementation in SPICE2, Static model of the real diode and its implementation in SPICE2, Large-signal model of the diode, Small-signal model of the diode, Temperature and area effects on the diode model parameters.	9
2	**Bipolar junction transistor :** Ebers-Moll static model, Ebers-Moll large signal mode , Ebers-Moll small signal model, Gummel – Poon static model, Temperature and area effects on the BJT model parameters. **Heterojunction Bipolar junction transistor (HBT):** SiGe HBT, Static operation and characteristics, HICUM level 2: Internal transistor model.	9
3	**The four terminal MOS structure:** strong inversion, complete symmetric strong inversion model, simplified symmetric strong inversion model, simplified source referenced strong inversion model. **MOS Transistor SPICE models:** Level 1 static model, level 2 static model,	9

	level 1 and level 2 large signal model, small signal model, effect of temperature on the model parameters. **MOSFET BSIM models:** BSIM1 model, parameter listing, BSIM1 static model, BSIM1 charge model.	
4	**MOSFET BSIM models:** BSIM1 model, parameter listing, BSIM1 static model, BSIM1 charge model. **Advanced semiconductor device modeling:** Tunnel FET: need of TFET, device structure, TFET modelling approach, modelling the surface potential source channel junction: pseudo 2D method, modelling drain current: constant polynomial term assumption, tangent line approximation. Modeling of novel unipolar devices: Device structures and principles of operation of FinFET, HEMT, TFET. Basic modeling concepts- …….	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Implement the static model of an ideal diode and a real diode in SPICE2 software, demonstrating the ability to set up and run simulations.	**K3**
CO2	Implement and simulate the Ebers-Moll and Gummel-Poon static models for BJTs in SPICE2, demonstrating practical application skills.	**K3**
CO3	Explain the differences between the complete symmetric strong inversion model, the simplified symmetric strong inversion model, and the simplified source-referenced strong inversion model for MOS structures.	**K2**
CO4	Explain the TFET modeling approach and the importance of modeling the surface potential at the source-channel junction.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**	**2**		**1**							
CO2	**3**	**2**	**2**		**1**							
CO3	**3**	**2**	**2**		**1**							
CO4	**3**	**2**	**2**									

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	COMPACT HIERARCHICAL BIPOLAR TRANSISTOR MODELING WITH HICUM	Michael Schroter	World Scientific	1/e, 2010
2	Semiconductor Device Modeling With SPICE	Giuseppe Massobrio	McGraw-Hill	2/e, 1993
3	Tunnel Field-Effect Transistors (TFET) Modelling and Simulation	Jagadesh Kumar Mamidala	John Wiley	1/e, 2017
4	Operation and Modelling of the MOS Transistor	Yannis Tsividis	Oxford University Press	3/e,2010

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	SEMICONDUCTOR DEVICES MODELLING AND TECHNOLOGY	Nandita Das Gupta	PHI learning	1e/2004
2	Semiconductor Device Modelling	Christopher M. Snowden	Springer	1e/2012
3	Semiconductors Physics and Devices	Donald Neamen	Tata Mc Graw Hill	4e/2017
4	Physics of Semiconductor Devices	S M Sze	Wiley	3e/2007

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117106033
2	https://nptel.ac.in/courses/117106033
3	https://nptel.ac.in/courses/117106033
4	https://www.youtube.com/playlist?list=PLbMVogVj5nJQ2k2HAGHFENB4a2nI8OppN

SEMESTER S6

SEMICONDUCTOR PACKAGING AND TESTING

Course Code	**PEEVT 637**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCECT302 Solid State Devices	**Course Type**	Elective

Course Objectives:

1. Understand the various semiconductor packaging techniques, including hermetic and plastic packaging, wire bonding, and flip-chip processes, as well as package form factors and standardizations.
2. Learn the principles and challenges of surface-mount technology, including the comparison of peripheral leads versus area array packages, and explore current and future trends in lead-free and halogen-free packaging.
3. Explore the packaging requirements for various applications, such as MEMS, image sensors, memory cards, and solar technology, and understand the role of copper interconnects and low-k dielectric materials in future packaging options.
4. Gain knowledge of reliability testing methodologies for semiconductor packages, including preconditioning, temperature cycling, thermal shock, and the limitations of current reliability testing techniques.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Semiconductor packaging: Introduction, Hermetic packaging, Plastic packaging, Wire bonding process flow, flip-chip process flow comparison, Equipment, Material interactions. Package form factors and families: Introduction, Package outline standardization, Leaded package families, Quad lead package family, Substrate-based package families, Chip scale packages, Stacked-die package, Package-on-package, Flip-chip packages, Wafer-level chip scale packages.	**9**

2	Surface-mount technology: Objectives, Introduction, Package cracking, Surface-mount packages: peripheral leads versus area array, Issues with advanced packaging, Current and future trends: Lead-free and halogen-free packaging.	**9**
3	Packaging needs: Introduction, Tape automated bonding, Micro electro-mechanical systems (MEMS), Package types used for MEMS, MEMS packaging examples, Image sensor modules, Memory cards, Packaging needs for solar technology. Copper interconnects and low-k dielectric materials. Dielectric constant requirements at each technology node. Future interconnect and dielectric materials. Future packaging options.	**9**
4	Package reliability: Reliability testing – Introduction, Background, Examples of reliability tests: Preconditioning, Package failure mode, Temperature cycling and thermal shock, High-temperature storage life, Temperature-humidity-bias tests, Limitations of reliability testing.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Describe and differentiate various semiconductor packaging techniques and identify package form factors and standardizations.	**K2**
CO2	Understand the principles of surface-mount technology, identify the challenges of advanced packaging, and recognize trends in lead-free and halogen-free packaging.	**K2**
CO3	Explain the packaging requirements for MEMS, image sensors, memory cards, and solar technology, and understand the importance of copper interconnects and low-k dielectric materials in future packaging solutions.	**K2**
CO4	Conduct and interpret various reliability tests for semiconductor packages, and understand the limitations and significance of these tests in ensuring package reliability.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**1**	**1**	**1**	**1**	**1**				**2**	**1**		**1**
CO2	**2**	**1**	**1**	**1**	**2**				**2**	**1**		**1**
CO3	**2**	**1**	**1**	**1**	**2**				**2**	**2**		**2**
CO4	**2**	**2**	**1**	**2**	**3**				**2**	**2**		**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Semiconductor Packaging – Materials Interaction and Reliability	Andrea Chen, Randy Hsiao-Yu Lo	CRC Press , Taylor & Francis Group	2012
2	Semiconductor Advanced Packaging.	John H Lau	Springer	2021
3	Microelectronic Packaging	Tummala, Rao R.	Springer	2001
4	Electronic Packaging and Interconnection Handbook	Charles A Harper	McGraw-Hill Professional	4th, 2004

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Advanced Electronic Packaging	Richard K. Ulrich, William D. Brown	Wiley-Interscience	2nd Edition, 2006
2	Chip Scale Package	John H. Lau, Ricky S.W. Lee	McGraw-Hill	2002
3	Electronic Packaging, Microelectronics, and Interconnection Dictionary	Charles Harper, Martin Miller	McGraw-Hill Education	2005

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/noc/courses/noc22/SEM1/noc22-me61/
2	https://archive.nptel.ac.in/courses/108/108/108108031/
3	https://www.youtube.com/watch?v=RpLnIiegXbg
4	https://www.youtube.com/watch?v=k2CognMJ_9I

SEMESTER S6

VLSI VERIFICATION & TESTING

Course Code	PEEVT635	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	ESE Marks	60
Credits	5/3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT402 Digital System Design	Course Type	5 Credit Elective

Course Objectives:

1. To understand the complexity of verification and build SoC verification environments.
2. To use UVM to develop scalable, reusable, and efficient verification environments for complex designs.
3. To gain proficiency in System Verilog for designing and verifying complex digital systems
4. To design and implement effective test strategies to detect and diagnose faults in VLSI circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction**: Scope of testing and verification in VLSI design process; Issues in testing and verification of complex chips; embedded cores and SOCs, Functional verification, Timing verification. **System Level Verification**: Test Plan-Block Level Verification-Interface Verification. Application Based Verification-Canonical SoC Design-Testbench for the Canonical Design. Fast Prototype vs. 100 Percent Testing - FPGA Prototyping, Emulation Based Testing, Silicon Prototyping. Gate Level Verification-Sign Off Simulation, Gate Level Simulation with Unit-Delay Timing , Gate Level Simulation with Full Timing. Formal Verification. Choosing Simulation Tools.	9

2	**Specialized Hardware for System Verification** - Accelerated Verification Overview, RTL Acceleration-Software Driven Verification, Traditional In Circuit Verification, Intellectual Property, Design Guidelines for Accelerated Verification. **UVM**: Introduction, Verification Planning and Coverage-Driven Verification, Multi-Language and Methodologies, UVM Overview, UVM Testbench and Environments, Interface UVCs, System and Module UVCs, Software UVCs, The SystemVerilog UVM Class Library, UVM Utilities. UVM Library basics, Interface UVCs, Automating UVC Creation, Simple Testbench Integration, Register and Memory Package, System UVCs and Testbench Integration.	9
3	**SystemVerilog**: Basic circuits design using SystemVerilog. Procedural Statements and Functions, Implementation of OOPs Concepts in System Verilog, SystemVerilog DPI (Direct Programming Interface), Example, Enum Cast, Code library, SystemVerilog TestBench-SystemVerilog TestBench and Its components, combinational circuit – TestBench Example, Memory Model – TestBench Example. Connecting the testbench and design. 4 port ATM Router- Case study.	9
4	**Testing:** VLSI testing process and test equipment, Automatic Test Equipment, SCOAP Controllability and Observability, High-Level Testability Measures, Combinational circuit test generation-Redundancy Identification (RID)-Combinational ATPG Algorithms-Test Generation Systems-Test Compaction, Sequential circuit test generation-ATPG for Single-Clock Synchronous Circuits-Simulation-Based Sequential Circuit ATPG, Memory Test, Delay Test, IDDQ test, Design for testability-DFT and Scan Design-Partial-Scan Design. Built-In-Self-Test (BIST)- Random Logic BIST, Memory BIST, Boundary Scan Standard, Analog Test Bus Standard.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

Criteria for Evaluation (Evaluate and Analyse): 20 marks

1. Literature Review and Report (10 Marks)

Assessment Method:

- Students select recent publications on a specific topic related to the course (eg. BIST).
- Preparation of a report summarizing the findings, discussing the significance, and proposing future research directions.

Criteria:

- Relevance of Chosen Publications (2 Marks): Selection of up-to-date and significant research papers.
- Depth of Analysis (4 Marks): Thorough understanding and critical analysis of the literature.
- Clarity and Organization (2 Marks): Well-structured report with clear arguments.
- Originality (2 Marks): Innovative insights or perspectives.

2. UVM for verification and Report (5 Marks)

Assessment Method:

- Use UVM for verification of digital circuits(eg. ALU Verification with UVM, Asynchronous FIFO) using ModelSim Questa/ Synopsys VCS/ Cadence Incisive Enterprise Simulator/ Xilinx Simulator (XSIM) or any other FOSS tools.
- Preparation of a detailed report.

Criteria:

- Comprehensiveness (2 Marks): Detailed explanation of the design and the tool used.
- Application Understanding (1 Mark): Insight into how the designing relate to the theoretical concepts covered in class.
- Report Quality (1 Mark): Clear and concise presentation of information.
- Reflective Analysis (1 Mark): Personal reflections and insights gained from the realization.

3. Simulation Tool Familiarization for SystemVerilog and Report (5 Marks)

Assessment Method:

- Students use/study simulation tools (e.g., using ModelSim Questa/ Synopsys VCS/ Cadence Incisive Enterprise Simulator/ Xilinx Simulator (XSIM) or any other FOSS tools) to model digital designs discussed in the course.
- They prepare a report on the simulations, including the methodology, results, and interpretations.

Criteria:

- Tool Knowledge (2 Marks): Understand the features of the simulation tool.
- Familiarisation of Simulations (1 Mark): Representation of design characteristics.
- Report Quality (2 Mark): Well-organized and clearly written report.

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Gain proficiency in industry standards and methodologies for design and verification for VLSI	**K2**
CO2	Create, configure and customize reusable, scalable, and robust UVM Verification Components (UVCs)	**K3**
CO3	Analyse the use of procedural statements and routines in testbench design with system verilog.	**K4**
CO4	Apply OOP concepts in designing testbench with system verilog	**K3**
CO5	Effectively test VLSI systems using existing test methodologies, equipments and tools.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**		**3**		**3**							
CO2	**3**		**3**	**3**	**3**							
CO3	**3**	**3**	**3**		**3**							
CO4	**3**		**3**	**3**	**3**							
CO5	**3**		**3**	**3**	**3**							

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	SystemVerilog for Verification	Chris Spears	Springer	2nd Edition, 2008
2	Digital Systems Testing and Testable Design	M. Abramovici, M. A. Breuer, A. D. Friedman	Piscataway, New Jersey: IEEE Press,	1994
3	Reuse Methodology Manual for System-on-a-Chip Designs	Micheal Keating & Pierre Bricaud	Springer	2002
4	A Practical Guide to Adopting Universal Verification Methodology (UVM)	Sharon Rosenberg & Kathleen A Meade	Lulu publishers (Lulu.com)	2nd Edition, 2012
5	The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology	Ray Salemi	Boston Light Press	2013
6	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits	M. Bushnell and V. D. Agarwal	Kluwer Academic Publishers	2000

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language, 10.1109/IEEESTD.2018.8299595	IEEE	IEEE	2018
2	Introduction to Formal Hardware Verification	T.Kropf	Springer	2000
3	System-on-a-Chip Verification-Methodology and Techniques	P. Rashinkar, Paterson and L. Singh	Kluwer Academic Publishers	2001
4	Principles of Testing Electronic Systems	Samiha Mourad and Yervant Zorian	Wiley	2000
5	SoC Verification Methodology and Techniques	Prakash Rashinkar & Peter Paterson	Springer	2007

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1, 2, 4	Design Verification and Test of Digital VLSI Circuits, https://archive.nptel.ac.in/courses/106/103/106103116/
2, 3	Unleashing SystemVerilog and UVM Video Series, Synopsys https://m.youtube.com/playlist?list=PLEgCreVKPx5AP61Pu36QQE0Pkni2Vv-HD

SEMESTER S6

DIGITAL SIGNALS AND PROCESSING

Course Code	PBEVT604	CIE Marks	60
Teaching Hours/Week (L: T:P: R)	3:0:0:1	ESE Marks	40
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Mathematics for Electrical and Physical Sciences (GYMAT101, GYMAT201)	Course Type	Theory

Course Objectives:

1. Understand the definitions and classifications of continuous and discrete-time signals, and perform basic operations on these signals, including analysing their frequency characteristics.
2. Comprehend the fundamental properties of continuous-time and discrete-time systems, with a focus on linear time-invariant (LTI) systems, their impulse responses, and various types of convolutions.
3. Gain proficiency in the Fourier transform for both continuous and discrete-time signals, understand the sampling theorem, and learn about frequency aliasing and the properties of the Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT).
4. Develop the ability to design and analyse digital FIR and IIR filters, understand their transfer functions and structures, and apply various methods for digital filter design.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to Continuous andDiscrete Time Signals:** Definition of signal, Basic continuous-time signals, Frequency and angular frequency, Basic operation on signals, Basic discrete-time signals - Frequency and angular frequency of discrete-time signals, Classification of continuous-time & discrete- time signals: Periodic and Non-periodic signals, Even and Odd signals, Energy and power signals.	9

2	**Systems:** System definition, Continuous-time and discrete-time systems, Properties – Linearity, Time invariance, Causality, Invertibility, Stability, Representation of systems using impulse response. Linear time invariant systems: LTI system definition, Response of a discrete-time LTI system and the convolutional sum, Circular convolution, Linear convolution through circular convolution, Correlation of discrete-time signals.	**9**
3	**Frequency analysis of signals:** Fourier transform of continuous-time and discrete-time signals, Parseval's theorem, Interpretation of Spectra,Sampling theorem (Proof not needed), Frequency aliasing due to sampling, Need for anti-aliasing filters, Discrete Time Fourier Transforms – properties, Discrete Fourier Transform – Properties -DFT as a linear transformation, IDFT, FFT-Radix-2 DIT and DIF algorithms, FFT Algorithms for IDFT.	**9**
4	**Digital Filters:** Digital FIR Filter, Transfer function - Difference equation, Linear phase FIR filter, Concept of windowing, Direct form and cascade realization. Digital IIR Filters – Transfer function, Difference equation, Direct and parallel Structures, Design of analog Butterworth filters, Analog frequency transformations, Impulse invariance method, Bilinear transformation, Analog prototype to digital transformations.	**9**

Suggestion on Project Topics

1. Collect various real-world signals (audio, temperature, ECG, etc.) and classify them into continuous-time and discrete-time signals. Perform basic operations such as scaling, shifting, and time-reversal on these signals and analyse their properties.

2. Generate discrete-time signals and compute their frequency components using the Discrete Fourier Transform (DFT). Analyse the frequency spectrum and compare it with the theoretical frequency components.

3. Capture audio signals using a microphone, classify them as continuous-time signals, and convert them into discrete-time signals. Perform operations like filtering, amplification, and noise reduction.

4. Obtain ECG signals, classify them, and perform basic operations to analyse heart rate variability, detect anomalies, and filter out noise.

5. Design a discrete-time linear time-invariant (LTI) system and determine its impulse response, then compute the output of the system for various input signals using convolution.

6. Analyse the properties (linearity, time-invariance, causality, and stability) of a given discrete-time system and provide theoretical justifications and practical demonstrations for each property.

7. Design and implement a digital equalizer for audio systems, utilizing the properties of linear time-invariant (LTI) systems. Analyse its performance in adjusting different frequency bands.

8. Develop a real-time noise cancellation system using digital filters, leveraging convolution and system properties. Test the system in various noisy environments.

9. Compute the Fourier transform of continuous-time and discrete-time signals and analyse their spectra. Use tools like MATLAB, Octave or Python for computation and visualization.

10. Investigate the effects of sampling on signal representation and design an anti-aliasing filter. Demonstrate the sampling theorem and implement the filter to prevent aliasing.

11. Design a spectrum analyser to monitor and analyse the frequency spectrum of wireless communication signals. Use Fourier transforms to visualize and interpret the spectral components.

12. Design and implement an anti-aliasing filter for digital image processing, ensuring high-quality image acquisition without aliasing effects.

13. Design a Finite Impulse Response (FIR) filter using the windowing method. Implement the filter in MATLAB, Octave or Python and analyse its frequency response.

14. Design an Infinite Impulse Response (IIR) filter using the bilinear transformation method. Compare its performance with an analog prototype and analyse stability and frequency response.

15. Design and implement a Finite Impulse Response (FIR) filter to improve audio signal quality in a music player. Analyse the filter's performance in real-time audio enhancement.

16. Design an Infinite Impulse Response (IIR) filter to optimize signal transmission in communication systems. Evaluate its performance in reducing noise and improving signal clarity.

Course Assessment Method
(CIE: 60 marks, ESE: 40 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Project	Internal Ex-1	Internal Ex-2	Total
5	30	12.5	12.5	60

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 2 marks **(8x2 =16 marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 2 sub divisions. Each question carries 6 marks. **(4x6 = 24 marks)**	**40**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Identify and classify continuous and discrete-time signals, analyse their frequency components, and perform basic operations on these signals.	**K2**
CO2	Demonstrate an understanding of the properties and representations of continuous-time and discrete-time systems, particularly focusing on linear time-invariant (LTI) systems and their impulse responses.	**K2**
CO3	Proficiency in applying Fourier transforms to continuous and discrete-time signals, interpreting spectra, understand the implications of the sampling theorem, and utilizing the properties of the Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT).	**K3**
CO4	Design and analyse digital FIR and IIR filters, understand their structures and transfer functions, and apply techniques such as impulse invariance and bilinear transformation for digital filter design.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	1	1				1	1	-	
CO2	2	1	1	1	1				1	1	-	
CO3	2	2	1	1	2				1	1	1	1
CO4	2	2	1	2	2				1	1	1	1

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Signal Processing: Principles, Algorithms& Applications	John G. Proakis, Dimitris G. Manolakis	Pearson,	4e, 2007
2	Signals and Systems	Simon Haykin , Barry Van Veen	Wiley	2e, 2007
3	Digital Signal Processing: A computer – based approach	Sanjit K. Mitra	McGraw Hill Education	4e, 2013
4	Signals and Systems,	A Anand Kumar	Prentice Hall India Learning Private Limited	3e, 2013

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Signal Processing	Monson Hayes	McGraw Hill Education	2e, 2009
2	Schaum's Outline of Signals and Systems	Hwei P. Hsu	McGraw Hill	4e, 2019
3	Signals And Systems	Sanjay Sharma	S K Kataria and Sons	2013

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/101/117101055/
2	https://archive.nptel.ac.in/noc/courses/noc20/SEM1/noc20-ee31/
3	https://onlinecourses.nptel.ac.in/noc20_ee15/preview
4	https://nptel.ac.in/courses/108106151

PBL Course Elements

L: Lecture (3 Hrs.)	**R: Project (1 Hr.), 2 Faculty Members**		
	Tutorial	**Practical**	**Presentation**
Lecture delivery	Project identification	Simulation/ Laboratory Work/ Workshops	Presentation (Progress and Final Presentations)
Group discussion	Project Analysis	Data Collection	Evaluation
Question answer Sessions/ Brainstorming Sessions	Analytical thinking and self-learning	Testing	Project Milestone Reviews, Feedback, Project reformation (If required)
Guest Speakers (Industry Experts)	Case Study/ Field Survey Report	Prototyping	Poster Presentation/ Video Presentation: Students present their results in a 2 to 5 minutes video

Assessment and Evaluation for Project Activity

Sl. No	Evaluation for	Allotted Marks
1	Project Planning and Proposal	5
2	Contribution in Progress Presentations and Question Answer Sessions	4
3	Involvement in the project work and Team Work	3
4	Execution and Implementation	10
5	Final Presentations	5
6	Project Quality, Innovation and Creativity	3
Total		**30**

1. **Project Planning and Proposal (5 Marks)**
    - Clarity and feasibility of the project plan
    - Research and background understanding
    - Defined objectives and methodology

2. **Contribution in Progress Presentation and Question Answer Sessions (4 Marks)**
    - Individual contribution to the presentation
    - Effectiveness in answering questions and handling feedback

3. **Involvement in the Project Work and Team Work (3 Marks)**
    - Active participation and individual contribution
    - Teamwork and collaboration

4. **Execution and Implementation (10 Marks)**
    - Adherence to the project timeline and milestones
    - Application of theoretical knowledge and problem-solving
    - Final Result

5. **Final Presentation (5 Marks)**
    - Quality and clarity of the overall presentation

- Individual contribution to the presentation
- Effectiveness in answering questions

6. **Project Quality, Innovation, and Creativity (3 Marks)**

    - Overall quality and technical excellence of the project
    - Innovation and originality in the project

Creativity in solutions and approaches

SEMESTER S6

DATA ANALYSIS

Course Code	OEEVT611	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To understand the basic concepts of data analytics.
2. To enable learners to perform data analysis on a real world scenario using appropriate tools.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Data Analysis - Analytics, Analytics Process Model, Analytical Model Requirements. Data Analytics Life Cycle overview. Basics of data collection, sampling, preprocessing and dimensionality reduction	9
2	Descriptive statistics - Measures of central tendency and dispersion, Association of two variables - Discrete variables, Ordinal and Continuous variable, Probability calculus - probability distributions, Inductive statistics - Point estimation, Interval estimation, Hypothesis Testing - Basic definitions, t- test	9
3	Supervised Learning - Classification, Naive Bayes, KNN, Linear Regression. Unsupervised Learning - Clustering, Hierarchical algorithms – Agglomerative algorithm, Partitional algorithms - K- Means. Association Rule Mining - Apriori algorithm	9
4	Big Data Overview – State of the practice in analytics, Example Applications - Credit Risk Modeling, Business Process Analytics.Big Data Analytics using Map Reduce and Apache Hadoop, Developing and Executing a HadoopMapReduce Program.	9

	Overview of modern data analytic tools.Data Analysis Using R - Introduction to R - R Graphical User Interfaces, Data Import and Export, Attribute and Data Types, , Exploratory Data Analysis - Visualization Before Analysis, Dirty Data, Visualizing a Single Variable, Examining Multiple Variables.	

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain the basic and mathematical concepts for data analytics **(CognitiveKnowledge Level: Apply)**	**K2**
CO2	Illustratevariouspredictiveanddescriptiveanalyticsalgorithms(**Cognitive Knowledge Level: Apply)**	**K3**
CO3	DescribethekeyconceptsandapplicationsofBigDataAnalytics**(Cognitive Knowledge Level: Understand)**	**K2**
CO4	Use R programming tool to perform data analysis and visualization	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**2**	**2**								**2**
CO2	**3**	**3**	**2**	**2**								**2**
CO3	**3**	**3**	**2**	**2**	**2**							**2**
CO4	**3**	**3**	**2**	**2**	**3**							**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Analytics in a Big Data World: The Essential Guide to Data Science and its Business Intelligence and Analytic Trends",	Bart Baesens	John Wiley & Sons,	2013.
2	EMC Education Services, Data Science and Big Data Analytics: Discovering, Analyzing, Visualizing and Presenting Data	David Dietrich	John Wiley & Sons,	2015.
3	Data Mining Concepts and Techniques'	Jaiwei Han, MichelineKamber	Elsevier,.	2006
4	Introduction to Statistics and DataAnalysis	Christian Heumann and Michael Schomaker	Springer,	2016

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Data Mining: Introductory and Advanced Topics.	Margaret H. Dunham,	Pearson,	2012.
2	Intelligent Data Analysis	Michael Berthold, David J. Hand	Springer	2007

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc21_cs45/preview
2	https://archive.nptel.ac.in/courses/106/107/106107220/

SEMESTER S6

ELECTRONIC HARDWARE FOR ENGINEERS

Course Code	OEEVT612	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To introduce students to the exciting field of electronic hardware designing and prototyping

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Review of Active and Passive Components Introduction to Brief History of Printed Circuits; What is PCB, Difference between PWB and PCB, Types of PCBs: Single Sided (Single Layer), Multi-Layer (Double Layer), PCB Materials Component Package Types Axial lead, Radial Lead, Single Inline Package(SIP), Dual Inline Package (DIP), Transistor Outline (TO), Pin Grid Array (PGA), Metal Electrode Face (MELF), Leadless Chip Carrier (LCC), Small Outline Integrated Circuit (SOIC), Quad Flat Pack(QPF) and Thin QFP(TQFP), Ball Grid Array (BGA), Plastic Leaded Chip Carrier (PLCC).	7
2	Brief History of EDA, Latest Trends in Market, How it helps and why it requires, Different EDA tools, Introduction to SPICE and PSPICE Environment, Introduction and Working of PROTEUS Introduction to PCB Design using OrCAD tool PCB Designing Flow Chart: Schematic Entry, Net listing, PCB Layout Designing, Prototype Designing, Design Rule Check(DRC), Design For Manufacturing(DFM) PCB Making: Printing, Etching, Drilling, Assembly of components Introduction to PCB Design using PROTEUS tool Assembly of simple circuits	10
3	Types of Product Testing Acceptance Testing, Type Testing , Safety Testing, Safety, safety standards, safety certificates (CE, UL and VDE), Effect of	10

	environmental testing(refer to IEC 60068-1 for guidance) Quality Standards General awareness of quality standards, quality management systems & documentation, Awareness on ISO 17025, ISO 9001, Calibration and Uncertainty of measurements, Awareness on disposal of Electronic waste. Testing Procedures: Switch Mode Power Supply - (Applicable Standard: IS 14886) Safety Testing(Earth Leakage current Test, Dielectric Test, Short Circuit Protection), Performance Testing (Line Regulation, Load Regulation for a variation of Load Min to Max load and vice versa. Safety Testing of Household Appliances: (Applicable Standard IS 302-1) Definitions and Terminology, Protection against Shock, Power Input and Current, Leakage Current and Electric Strength at Operating Temperature	
4	Assembly and Maintenance of PC: Introduction to Computer - Difference between Hardware & Software, booting concept, Different input and output devices/ cables, connectors, different types of motherboard, controller cards, Ethernet cards, Different types of RAM used in PC's. Installation: BIOS setting, Formatting of Hard Disk, Installation of Windows, Off-line drive installation / online drive installation / Windows file repairing / BIOS password break / Administrative password break / Data recovery. Application Software Installation, Dual Booting Installation. Assembly and dismantling: Assembly and dismantling of PCs front panel connection, servicing of computer, Type of Backup, Taking Backup files and fine tuning the system, running diagnostics tool, running of virus protection program.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Identify various electronic components along with their specifications.	K2
CO2	Design PC Busing modern software tools.	K3
CO3	Explain various testing procedures of electronic products.	K2
CO4	Experiment and debug various software and hardware issues of a PC.	K3

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3											**3**
CO2	3	2	2	**3**	3							**3**
CO3	3	2	2	**3**	**3**							**3**
CO4	3	3	2	**3**	3							**3**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	PCB Designer´s Reference.	C. Robertson.	Prentice Hall,	2003
2	Signal Integrity Issues and Printed Circuit Board Design,	D. Brooks,	Prentice Hall	2003
3	Advances in Electronic Testing,	D Gizopoulos,	Springer	2006

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Printed Circuits Handbook,	C. Coombs,	McGraw-Hill Professional,	6 edition, 2007.
2	Electronic Testing Handbook,		McGraw-Hill,	Dec 1993
3	PC Repair and Maintenance, A Practical Guide,	Joel Rosenthal, Kevin Irwin		, 2003
4	Simple Guide to Computer Maintenance &Troubleshooting,	AdaneNegaTarekegn, AlemuKumilachewTegegne,		2015

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://elearn.nptel.ac.in/shop/iit-workshops/completed/electronic-hardware-design-where-to-start/
2	https://onlinecourses.nptel.ac.in/noc22_ee25/preview
3	https://nptel.ac.in/courses/117103148

SEMESTER S 6

POWER ELECTRONICS

Course Code	**OEEVT613**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Analog Circuits (PCECT303)	**Course Type**	Theory

Course Objectives:

1. To study the characteristics of power electronic devices.
2. To study different power converter circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction:** Scope and applications of Power Electronics, Properties of ideal switch. **Structure and static characteristics:** Power diodes, Power BJT, Power MOSFET & IGBT – comparison. Basic principles of wide band gap devices – SiC & GaN. **Safe Operating Area:** Power BJT, Power MOSFET & IGBT. **Drive Circuits:** Power BJT and Power MOSFET (any two example circuits – no analysis).	**9**
2	**SCR:** Structure, two transistor analogy, static characteristics. **Rectifiers:** Three phase diode bridge rectifiers, Single phase half controlled rectifier with R load – Single phase fully controlled bridge rectifier (continuous conduction) – output voltage equation. Principle of three phase half wave controlled rectifier– (average output voltage equation for continuous load current) – related simple problems (1-phase & 3-phase).	**9**
3	**DC – DC Switch Mode Converters:** Buck, Boost and Buck-boost DC-DC converters. Waveforms and expression of DC-DC converters for output voltage, voltage and current ripple under continuous conduction mode. **Isolated converters:** Flyback, Forward, Push Pull, Half bridge and Full	**9**

	bridge converters – Waveforms and governing equations.	
4	**DC-AC Switch Mode Inverters:** Inverter topologies, Driven Inverters: Push-Pull, Half bridge and Full bridge configurations, Single phase PWM inverters (Single pulse width and sinusoidal pulse width modulation) – rms output voltage equation and output voltage waveforms.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Outline the operation of power semiconductor devices and its characteristics.	**K2**
CO2	Design and analyze various rectifier circuits for power devices	**K3**
CO3	Analyze different power converter circuits	**K3**
CO4	Illustrate different types of inverter circuits	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3											2
CO2	3		3		3	3						2
CO3	3		3	3	3	3	3					2
CO4	3		3	3	3	3	3					2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Power Electronics Essentials & Applications	L Umanand	Wiley India	Reprint Edition 2014
2	Power Electronics Circuits, Devices, and Applications	Muhammad H Rashid	Pearson India	Third Edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Power Electronics Converters, Applications, and Design	Ned Mohan, Tore M Undeland, William P. Robbins	Wiley India	Third Edition
2	Power Electronics Principles and Applications	Joseph Vithayathil	Tata McGraw-HILL	Second Reprint 2010
3	Power Electronics	Daniel W Hart	McGraw-HILL	2011
4	SiC and GaN Wide Bandgap Device Technology Overview,	Milligan, J. W., Sheppard, S., Pribble, W., Wu, Y.-F., Muller, G., &Palmour, J. W	2007 IEEE Radar Conference.	doi:10.1109/radar.2007.374395.

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://www.youtube.com/watch?v=fOZ8bUrFJGk
2	https://archive.nptel.ac.in/courses/117/108/117108124/
3	https://www.youtube.com/watch?v=Dg5AIy0bY1A

SEMESTER S6

ENTREPRENEURSHIP

Course Code	OEEVT614	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To understand the importance of entrepreneurship and apply it in an organization.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Entrepreneurship: definition, requirements to be an entrepreneur, entrepreneur and intrapreneur, entrepreneur and manager, growth of entrepreneurship in India, women entrepreneurship, rural and urban entrepreneurship. Entrepreneurial Motivation: motivating factors, motivation theories-Maslow's need hierarchy theory, McClelland's acquired need theory, government's policy actions towards entrepreneurial motivation, entrepreneurship development programmes.	9
2	Types of Enterprises and Ownership Structure: small scale, medium scale and large scale enterprises, role of small enterprises in economic development; proprietorship, partnership, limited companies and co-operatives: their formation, capital structure and source of finance. Institutional Support and Policies: institutional support towards the development of entrepreneurship in India, technical consultancy organizations, Government programs, policies, incentive and institutional networking for enterprise setting.	9
3	Projects: identification and selection of projects, project report, contents and formulation, elements of project formulation, project design and network analysis, concept of project evaluation, methods of project evaluation: internal	9

	rate of return method and net present value method.	
4	Management of Enterprises: objectives and functions of management, scientific management, general and strategic management; introduction to human resource management: planning, job analysis, training, recruitment and selection, marketing and organizational dimension of enterprises; enterprise financing, raising and managing capital, shares, debentures, bonds, cost of capital; break- even analysis, balance sheet analysis.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Describe the fundamental concepts of entrepreneurship	K1, K2, K3
CO2	Understand entrepreneurial motivation and motivation theories	K1, K2, K3
CO3	Analyze types of enterprises and ownership structure	K1, K2, K3
CO4	Apply project evaluation methods	K1, K2, K3, K4, K5
CO5	Evaluate enterprise financial strength	K1, K2, K3, K4, K5

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1										1	1	
CO2								2		1		
CO3										1		
CO4	2		1		2					1	3	
CO5	2		1		2					1	3	

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Entrepreneurial Development,	Khanka,SS	S Chand & Company Ltd. New Delhi	2007
2	Entrepreneurial Development	Ram Chandran	Tata McGraw Hill, New Delhi	2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Entrepreneurial Development Programmes and Practices	Saini, J. S	Deep & Deep Publications	,2012
2	Entrepreneurship for Engineers	Badhai, B	Dhanpat Rai & co	2006
3	Project Management and Entrepreneurship	Desai,Vasant	HimalayanPublishing ,Mumbai	2017
4	Entrepreneurial Development	Gupta, Srinivasan	S Chand & Sons, New Delhi	2020

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/110106141
2	https://nptel.ac.in/courses/110106141
3	https://nptel.ac.in/courses/110106141
4	https://nptel.ac.in/courses/110106141

SEMESTER 6

BIOMEDICAL ENGINEERING

Course Code	OEETVT615	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. This course will introduce aspects of biomedical engineering as applied to biological systems described using engineering principles and the use of modern diagnostic and therapeutic equipment.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Physiology and Bio- Electric Concepts** Cell and their structure, Transport of ions through the cell membrane, Resting and action potentials, Bio-electric potentials. Electrode theory – Electrode potential, Types of electrodes, Equivalent circuit. Instrumentation amplifier, Isolation amplifier, Chopper amplifier, Devices to protect against electrical hazards.	9
2	**Body Potential Measurement** ECG – Nature of ECG waveform, ECG lead configurations, ECG recorder. EEG – Evoked potentials, Brain waves, Analysis of EEG EMG – Recording setup ERG and EOG	9
3	**Prosthesis** Heart Lung machine – Model of the heart-lung machine. Kidney machine – Dialysis.	9

	Nerve stimulators – Diagnostic/ Therapeutic stimulator. Centralized & Bedside monitoring Microprocessor based ventilator	
4	**Medical Imaging** Computer Tomography – Basic principle, Image construction, Block diagram, Applications. Magnetic Resonance Imaging – Block diagram, Image reconstruction. Ultrasonic Imaging – Different modes. Positron Emission Tomography – Principle.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
● 2 Questions from each module. ● Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	● Each question carries 9 marks. ● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Learn the basics of bioelectric potentials	**K1**
CO2	Understand the operation of different biopotential recorders	**K2**
CO3	Learn the medical equipment for diagnosis and therapy	**K1**
CO4	Understand the general concepts of imaging systems	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**										**2**
CO2	**3**	**2**										**2**
CO3	**3**	**3**										**2**
CO4	**3**	**3**										**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Handbook of Biomedical Instrumentation	R S Khandpur	TATA McGRAW HILL	
2	Biomedical Instrumentation and Measurements	Leslie Cromwell, Fred J Weibell, Erich A Pfeiffer	PHI	

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Medical Instrumentation Application and Design	John G Webster	WILEY	
2	Introduction to Biomedical Equipment Technology	Joseph J Carr, John M Brown	PEARSON	

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://www.youtube.com/watch?v=OqNDFF1RsMU
2	https://www.youtube.com/watch?v=mK6sPBbChqc
3	https://onlinecourses.swayam2.ac.in/nou23_bt05/preview
4	https://onlinecourses.nptel.ac.in/noc22_bt56/preview

SEMESTER S6

ANALOG IC DESIGN LAB

Course Code	PCEVL607	CIE Marks	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	ESE Marks	50
Credits	2	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PCECL303-Analog Circuits PCEVT601 - Analog CMOS Design	Course Type	PCL

Course Objectives:

1. Acquire skills in analog circuit design and analysis.
2. To familiarize students with EDA tools for simulation of analog integrated circuits.

Expt. No.	Experiments
1	Study the transfer characteristics of a MOSFET (n-MOS and p-MOS) and determine the threshold voltage.
2	Study the output characteristics of a MOSFET (n-MOS, p-MOS).
3	Study the effect of substrate potential on the threshold voltage and I-V characteristics of a MOSFET.
4	Design a CS amplifier with resistive load and triode load. Perform Transient, DC, and AC analyses, plot the frequency response, and obtain the bandwidth.
5	Design a CS amplifier with diode-connected load and constant current source load. Perform Transient, DC, and AC analysis, plot the frequency response, and obtain the bandwidth.
6	Design a Common Drain amplifier and perform AC analysis.
7	Design a Common Gate amplifier for a specified current gain and perform AC analysis.
8	Design a RC coupled amplifier using MOSFET and perform AC analysis.

9	Design a current mirror with passive and active loads.
10	Design a cascode current mirror with active and passive loads.
11	Design a differential amplifier for a specified gain and perform transient analysis.
12	Perform the layout design of a Common Source amplifier and check DRC and LVS.
13	A/D Converters - 3-bit Flash ADC
14	D/A converter - 3-bit Ladder type
15	Study of PLL: free running frequency lock range capture range

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	**15**	**10**	**10**	**5**	**50**

- ***Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.***
- ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Analyse single stage amplifiers and evaluate its characteristics.	**K4**
CO2	Design various circuits such as current mirrors, differential amplifiers.	**K5**
CO3	Outline various architectures of Data converters.	**K2**
CO4	Understand the concepts of layout generation of analog circuits.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3		3		1				2		1	
CO2	3		3	3	2				2		1	
CO3	3				2				2		1	
CO4	3				3				2		1	

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design of Analog CMOS Integrated Circuits	Behzad Razavi	McGraw-Hill Education	2nd Edition 2015
2	CMOS Analog Circuit Design	Philip E. Allen and Douglas R. Holberg	Oxford University Press	2nd Edition 2010
3	Analysis and Design of Analog Integrated Circuits	Hurst, S. Lewis and R. G. Meyer, WilePaul R. Gray, Paul Jy	Wiley	5th Edition 2010

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Analog Integrated Circuit Design	David A. Johns, Ken Martin	Wiley	2nd Edition 2013
2	CMOS: Circuit Design, Layout and Simulation	Baker, Li, and Boyce	Wiley	1st Edition 2009
3	Introduction to PSpice Using Orcad for Circuits and Electronics	M. H. Rashid	Pearson	3rd Edition 2003
4	Linear Integrated Circuits	D. Roy Choudhary, Shail B Jain	New Age International Books	3rd Edition 2021

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106030/
2	https://onlinecourses.nptel.ac.in/noc22_ee37/preview
3	https://www.youtube.com/@InderjitSingh87

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.

- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. **Lab Reports and Record Keeping (6 Marks)**

    - Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
    - Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

    - Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

    - Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
    - Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
    - Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
    - Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

    - Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. **Result with Valid Inference/Quality of Output (10 Marks)**

    - Accuracy of Results: Precision and correctness of the obtained results.

- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. **Viva Voce (10 Marks)**

    - Ability to explain the experiment, procedure results and answer related questions
    - Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. **Record (5 Marks)**

    - Completeness, clarity, and accuracy of the lab record submitted

SEMESTER 7

ELECTRONICS ENGINEERING

(VLSI DESIGN AND TECHNOLOGY)

SEMESTER S7

LOW POWER VLSI DESIGN

Course Code	PEEVT741	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To impart knowledge on different sources of power dissipation, power minimization techniques, switched capacitance minimization and working principle of adiabatic logic circuits

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Physics of Power dissipation in MOSFET devices** Need for low power circuit design, MIS Structure **Deep submicron transistor design issues: Short channel effects** Channel Length Modulation , Surface scattering, Punch through, Velocity saturation, Impact ionization, Hot electron effects, Body Effect, Narrow width effect, V_{th} roll-off, Drain Induced Barrier Lowering, Gate Induced drain leakage, Tunneling Through Gate Oxide, Subthreshold Leakage Current, **Emerging Technologies for Low Power:** Hi-K Gate Dielectric, Lightly Doped Drain–Source, Silicon on Insulator,	9
2	**Sources of power dissipation in digital ICs** – **Dynamic Power Dissipation:** Short Circuit Power: Short Circuit Current of Inverter , Short circuit current dependency on input rise and fall time, Variation of shortcircuit current with load capacitance. Switching power dissipation: Switching Power of CMOS Inverter, Switching activity and its effects.	9

	Glitching Power: Glitches and its effect on power dissipation **Static Power Dissipation:** Sources of Leakage Power, Effects of V_{dd} and V_t on speed, Constraints on V_t Reduction.	
3	**Low-Power Design Approaches-** **Supply Voltage Scaling for Low Power:** Effect of Supply voltage on Delay and Power Effect of Supply voltage on Static and Dynamic Power Multi VDD ,Dynamic VDD, Dynamic Voltage and Frequency Scaling (DVFS) Approaches. Architectural Level Approaches: Pipelining and Parallel Processing **Leakage power reduction Techniques:** Effect of threshold voltage on Leakage Power Transistor stacking, MTCMOS, VTCMOS Power gating& Clock gating Techniques.	**9**
4	**Circuit Design Styles for Low Power-** **Non clocked circuit design style:** Fully Complementary logic. NMOS and Pseudo –NMOS logic, Differential Cascode Voltage Switch logic(DCVS) **Clocked design style:** Basic concept, Dynamic Logic, Domino logic, Differential Current Switch Logic. **Adiabatic switching** – Adiabatic charging, Adiabatic amplification, Adiabatic logic gates, Pulsed power supplies.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Describe the impact of technology scaling on power dissipation in digital ICs and various short channel effects	K2
CO2	Discuss the different sources of power dissipation in digital ICs.	K2
CO3	Describe the various approaches for power management in digital ICs.	K2
CO4	Apply various clocked and non-clocked design styles for logic implementation	K3
CO5	Describe the use of Adiabatic switching for power management in digital ICs.	K2

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**											**2**
CO2	**3**											**2**
CO3	**3**			**2**								**2**
CO4	**3**	**2**	**3**		**3**							**2**
CO5	**3**											**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design of Analog CMOS Integrated Circuits	Behzad Razavi	McGraw-Hill	2/e, 2002
2	CMOS: Circuits Design, Layout and Simulation,	Baker, Li, Boyce,	Prentice Hall India,	2000
3	Microelectronic Circuits	Sedra & Smith	Oxford University Press	6/e,2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design,	Phillip E. Allen, Douglas R. Holbery	Oxford University Press	3/e
2	Fundamentals of Microelectronics	Behzad Razavi	Wiley student Edition	2014
3	Analysis and Design of Analog Integrated Circuits	Meyer Gray , Hurst, Lewis	Wiley	5/e, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
2	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
3	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
4	Switching Circuits and Logic Design by Prof. Indranil Sengupta Lectures 47-51

SEMESTER S7

INTRODUCTION TO MEMS

Course Code	PEEVT742	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Nil	Course Type	PE

Course Objectives:

1. Acquire a thorough understanding of MEMS products, micro fabrication evolution, and multidisciplinary applications including micro sensors and actuators.
2. Gain proficiency in MEMS material selection, fabrication techniques, and micro system packaging design considerations**.**

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	MEMS and Microsystems: Typical MEMS and microsystem products – Evolution of Microfabrication - Microsystem and microelectronics - Multidisciplinary nature of MEMS – Applications of Microsystems in Automotive Industry - Principles and examples of Micro sensors and micro actuators – micro accelerometer, Micro grippers, micro motors, micro valves, micro pumps.	**9**
2	Actuation and Sensing techniques: Actuation using Thermal forces, Actuation using Shape Memory Alloys, Actuation using Piezoelectric crystals, actuation using Electrostatic forces; Microsensors - Acoustic wave sensors, Biomedical sensors and biosensors, chemical sensors, pressure sensors, optical sensors - microfluidics.	**9**
3	Engineering science for Microsystem design - Atomic structure of Matter - Ions & ionization - Molecular Theory of matter & Intermolecular forces - Doping of semiconductors - Diffusion process - Electrochemistry - Quantum physics. Materials for MEMS and Microsystems - Substrate and wafer - Silicon as substrate Material - Silicon compounds - Silicon peizoresistors - Gallium Arsenide - Quartz - Peizoelectric crystals - Polymers.	**9**

4	Overview of Microsystem fabrication – Photolithography – Ion implantation-Diffusion – Oxidation – Chemical vapour deposition – Etching. Overview of Micro manufacturing – Bulk micro manufacturing, Surface micro machining , LIGA process. Micro system Packaging: general considerations in packaging design – Levels of Micro system packaging.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the basic concepts of MEMS and microsystem products.	**K2**
CO2	Understand the working principles of micro sensors and actuators.	**K2**
CO3	Identify the typical materials used for fabrication of micro systems.	**K2**
CO4	Illustrate the various methods in microsystem fabrication and micro manufacturing.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO31	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2										3
CO2	3	2										3
CO3	3	2	1									3
CO4	3	2	1									3

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	MEMS and Microsystems Design, Manufacture and Nanoscale Engineering	Tai-Ran Hsu,	Wiley	2nd , 2020
2	Foundations of MEMS	Chang Liu	Pearson	2nd , 2012
3	Microsystem Design	Stephen D Senturia	Springer	3rd, 2013

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Silicon VLSI Technology	James D Plummer	Prentice Hall	4th, 2012
2	MEMS	Nitaigur Premchand Mahalik	Tata Mc Graw Hill	2013
3	Micro and Nano Fabrication: Tools and Processes	Hans H. Gatzen	Springer	2015

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	NPTEL course : "MEMS & Microsystems" by Prof. Santiram Kal, Video Lecture No: 5, MEMS materials https://archive.nptel.ac.in/courses/117/105/117105082/
2	NPTEL course: "MEMS & Microsystems" by Prof. Santiram Kal, Video Lecture No: 13, Surface & Quartz Micromachining. https://archive.nptel.ac.in/courses/117/105/117105082/

SEMESTER 7

ADAPTIVE SIGNAL PROCESSING

Course Code	PEEVT 743	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBEVT 604	Course Type	Theory

Course Objectives:

1. Explain the role and importance of adaptive signal processing in communications signal processing
2. List and apply the various mathematical models to adaptive signal processing

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Adaptive systems: Definitions and characteristics - applications – properties examples - adaptive linear combiner input signal and weight vectors - performance function-gradient and minimum mean square error - introduction to filtering smoothing and prediction - linear optimum filtering-orthogonality - Wiener – Hopf equation-performance surface	9
2	Searching performance surface-stability and rate of convergence: Learning curve gradient search - Newton's method - method of steepest descent - comparison - Gradient estimation - performance penalty - variance - excess MSE and time constants – mis-adjustments	9
3	LMS/Newton algorithm - properties - sequential regression algorithm - adaptive recursive filters - random-search algorithms - lattice structure - adaptive filters with orthogonal signals.	9
4	Applications-adaptive modelling and system identification: Multipath communication channel, geophysical exploration, FIR digital filter synthesis	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Devise filtering solutions for optimising the cost function indicating error in estimation of parameters and appreciate the need for adaptation in design.	**K1**
CO2	Remember the performance of various methods for designing adaptive filters through estimation of different parameters of stationary random process clearly considering practical application specifications	**K2**
CO3	Understand convergence and stability issues associated with adaptive filter design and come up with optimum solutions for real life applications taking care of requirements in terms of complexity and accuracy	**K1**
CO4	Design and implement filtering solutions for applications such as channel equalisation, interference cancelling and prediction considering present day challenges.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**										
CO2	**3**	**3**										
CO3	**3**	**3**										**2**
CO4	**3**	**3**										

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Adaptive Signal Processing	Bernard Widrow and Samuel D. Stearns	Person Education	1985

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Adaptive Filter Theory	Simon Haykin	Person Education	2003
2	Theory and Design of Adaptive Filters	John R. Treichler, C. Richard Johnson, Michael G. Larimore	Prentice-Hall of India	2002

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/ya0-S1apej8?si=aaGBqDeR13YEa-67
2	https://youtu.be/xFQsSn0IVUQ?si=hm4Ow6n43XWx0LiR
3	https://youtu.be/AWcl2as6N1E?si=5dQbSh6smFOJrJn7
4	https://youtu.be/8fq02jEq2lY?si=aMPFYAdEH97V24xf

SEMESTER S7

HIGH SPEED INTEGRATED CIRCUITS

Course Code	**PEEVT 744**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT503 VLSI Technology	**Course Type**	Theory

Course Objectives:

1. Understand the fundamental principles of high-speed circuit operation, including signal integrity and the impact of transmission lines on high-speed signals.
2. Develop the ability to design high-speed digital circuits with a focus on clocking, timing analysis, and interconnect design, while optimizing for low power consumption.
3. Gain proficiency in designing high-speed analog components such as amplifiers, comparators, and phase-locked loops, with an emphasis on performance and jitter reduction.
4. Acquire knowledge of advanced design techniques for ensuring signal integrity, high-speed memory design, and the testing and verification of high-speed integrated circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Fundamentals of High-Speed Circuit Design Introduction to High-Speed ICs: Importance and applications of high-speed circuits in modern technology, Basic principles of high-speed operation. Signal Integrity: Understanding signal degradation, reflections, and crosstalk, Transmission lines and their impact on signal integrity, Impedance matching and termination techniques. High-Speed CMOS Circuits: Overview of CMOS technology for high-speed applications, Speed-power trade-offs and optimizing performance.	**9**

2	High-Speed Digital Design Techniques Clocking and Timing Analysis: Clock distribution networks and clock skew, Setup and hold times, timing margins. Jitter and its impact on timing accuracy. Interconnect Design: On-chip interconnects: RLC effects and delay modelling, Crosstalk minimization and signal buffering, Advanced interconnects: Optical and 3D interconnects. Low-Power High-Speed Design: Techniques for reducing power consumption in high-speed circuits, Voltage scaling, dynamic voltage, and frequency scaling (DVFS), Power gating and multi-Vt techniques.	**9**
3	High-Speed Analog Design High-Speed Amplifiers and Comparators: Design of wideband amplifiers: Gain-bandwidth trade-offs, Current-mode logic (CML) circuits for high-speed applications, Comparator design and optimization for speed. Phase-Locked Loops (PLL) and Clock Recovery Circuits: Basics of PLLs, Operation and applications, Design of PLL components: VCO, frequency dividers, phase detectors. Techniques for jitter reduction in PLLs. High-Speed Data Converters: Overview of ADCs and DACs in high-speed applications, Design challenges in high-speed data conversion, Techniques for enhancing the performance of data converters.	**9**
4	Module 4: Advanced Topics in High-Speed IC Design Design for Signal Integrity: Techniques for mitigating signal integrity issues, ESD protection and layout considerations for high-speed ICs, Packaging and PCB considerations in high-speed design. High-Speed Memory Design: SRAM, DRAM, and non-volatile memory technologies for high-speed applications, Memory interface design and timing considerations, Emerging memory technologies: MRAM, RRAM, etc. Testing and Verification of High-Speed Circuits: Techniques for testing high-speed digital and analog circuits, Signal integrity testing, eye diagrams, and bit error rate (BER) testing, Design for testability (DFT) and built-in self-test (BIST) methods.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	understand signal integrity issues in high-speed circuits and apply concepts of transmission lines and impedance matching effectively.	**K2**
CO2	design and optimize high-speed digital circuits, considering timing constraints, power consumption, and interconnect challenges.	**K3**
CO3	design high-speed analog components, such as amplifiers and PLLs, with a focus on achieving high performance and minimizing jitter.	**K3**
CO4	apply advanced techniques for ensuring signal integrity, designing high-speed memory systems, and performing thorough testing and verification of high-speed ICs.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	1	1	1				1	1	
CO2	2	2	2	1	2	1				1	1	1
CO3	2	2	2	1	2	1				2	1	1
CO4	2	3	3	2	1	1				2	1	2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages	Brian Young	Prentice Hall Modern Semiconductor Design	2000
2	Design of High-Performance Microprocessor Circuits	Anantha Chandrakasan, William J. Bowhill, Frank Fox	Wiley-IEEE Press	2000
3	High Speed Digital Design: A Handbook of Black Magic	Howard Johnson, Martin Graham	Prentice Hall Modern Semiconductor Design	1993
4	CMOS: Circuit Design, Layout, and Simulation	R. Jacob Baker	IEEE Press Series on Microelectronic Systems	2019

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting	Kyung Suk Oh, Xingchao Yuan	Prentice Hall Modern Semiconductor Design Series	2011
2	Signal Integrity and Radiated Emission of High-Speed Digital Systems	Spartaco Caniggia, Francescaromana Maradei	Wiley	2008
3	Advanced Signal Integrity for High-Speed Digital Designs	Stephen H. Hall, Howard L. Heck	Wiley	2008
4	High-Speed Circuit Board Signal Integrity	Stephen C Thierauf	Artech House	2017

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/108105375
2	https://onlinecourses.nptel.ac.in/noc24_ee134/preview
3	https://archive.nptel.ac.in/courses/117/106/117106030/
4	https://nptel.ac.in/courses/106103016

SEMESTER 7

EMBEDDED NETWORKS

Course Code	PEEVT 746	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0: 0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBEVT 504	Course Type	Theory

Course Objectives:

1. To understand Basic Network Architectures and familiarize with network protocols

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Distributed Embedded System**- Basic Network Architectures: Client-Server, Peer-to-Peer, Network Topologies**,** Basic concepts and definitions of LAN, WLAN, WAN &WPAN. OSI and ISO Models in Distributed Embedded Systems**.** Challenges in Designing Distributed Embedded Systems. Examples and applications of distributed embedded systems. **Embedded network protocol** CAN- CAN identifier, different layers, bit encoding, message format, Bus length, baud rate, Arbitration mechanism, Error control, Controller Architecture, Applications, and examples.	**7**
2	**Ethernet protocol**: Networking Devices-Routers, switches, hubs, and bridges, Ethernet protocol- Features, Frames, MAC, CSMA/CD -Principle, Back-off mechanisms. **Internet protocol**- Higher level protocols -TCP and UDP, IP packet structure- IPv4 and IPv6, Wireless LAN Configurations -Single-cell and multicell, Infrastructure and AdHoc mode, IEEE 802.11 MAC protocol.	**10**

	Nomadic Access- IEEE 802.11k. **Bluetooth Protocol**: Bluetooth Architecture, Bluetooth network topologies -Piconet and Scatternet. Bluetooth WPAN protocols- LMP and L2CAP, Bluetooth packet format-Classic packet & BLE format. Polling mechanism, Establishing a connection, Power saving modes, Bluetooth applications, Overview of Mobile Ad hoc networks (MANETs) & Vehicular Ad Hoc Networks (VANETs).	
3	**Sensor networking**: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing. **Operating system basics: Functions** of OS, Kernel, types of operating systems. Introduction to Real-time operating systems: Tasks, process, threads, multiprocessing and multitasking, task scheduling, task communication.	**7**
4	**Introduction to IoT and IoT networking:** devices vs. computers, technical building blocks, Basics of IoT networking, M2M area network, Modbus, ZigBee-Zigbee Architecture- LoRaWAN -Standardization and Alliances. **Introduction to cloud computing**: Data Collection, storage, and computing using a Cloud Platform (Basics Only).	**7**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination- 1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub-divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course, students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand basic distributed embedded systems architectures, topologies, and protocols.	**K2**
CO2	Understand the architectures, and principles of operation of ethernet, IP, and Bluetooth.	**K2**
CO3	Understand the concepts of sensor networking and RTOS	**K2**
CO4	Comprehend the concepts of IOT networking and cloud computing	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**		**3**	**3**								**2**
CO2	**3**	**2**	**3**	**3**								**2**
CO3	**3**		**3**	**3**								**2**
CO4	**3**	**2**	**3**	**3**								**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Embedded Systems Design: A Unified Hardware/Software Introduction.	Frank Vahid, Tony Givargis	John & Wiley Publications	2002
2	"Protocols and Architectures for Wireless Sensor Networks"	Holger Karl and Andreas Wiilig	John Wiley & Sons Limited 2008	2008
3	Operating systems Concepts	Abraham Silber Chatz, Peter Baer Galvin, Greg Gagne	Wiley Publications	
4	Internet of Things -Architectures and Design Principles	Raj Kamal	MacGraw Hill India Private Limited	

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Embedded Ethernet and Internet Complete	Jan Axelson	Penram Publications, 2003.	2003
2	"A Survey on Sensor Networks",	I.F. Akyildiz and Weillian	IEEE Communication Magazine	Aug 2007
3	Embedded systems an integrated approach	Lyla B Das	pearson	Ist edn
3	IoT fundamentals- networking technologies, protocol, and use cases.	David Hanes, Gonzalo Salgueiro et al.	Cisco Press	2017
4	Computers as Components: Principles of Embedded Computing System Design.	Wayne Wolf	Morgan Kaufman Publishers - Elsevier	3ed 2008

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/106/105/106105193/
2	https://nptel.ac.in/courses/108105057
3	https://onlinecourses.nptel.ac.in/noc24_cs24/preview
4	https://youtube.com/playlist?list=PLDD18E950D85E018C&si=6wnLOHy0GarETWi1

SEMESTER S7

FLEXIBLE ELECTRONICS

Course Code	**PEEVT 747**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Solid State Devices	**Course Type**	Theory

Course Objectives:

1. Identify the advantages, drawbacks, performances, complementarity, and uniqueness of large area manufacturing vs. silicon technology
2. Integrate the operation principles, architectures, and processing of main devices and systems fabricated for flexible electronics.
3. Predict systems integration issues and propose methods for integration and encapsulation of printed devices and systems.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Flexible and Printed Electronics: Evolution of Flexible Electronics, review of cutting edge research on electronics that can be flexible, plastic, stretchable, conformable or printed. Electronic materials, components, and systems, applications for IoT.	**9**

2	Materials, Processing, and Manufacturing: Various semiconductors, dielectric, and conducting materials, Organic semiconductors, from chemical bonds to bands, Charge injection and transport, Examples of printable functional materials, Thin-film Deposition and Processing Methods for Flexible Devices, Solution-based Patterning Processes; Ink-jet printing, gravure, and other processes, surface energy effects, multilayer patterning	**9**
3	Flexible Thin-Film Transistors and Circuits: Thin-Film Transistor; Device structure and performance, Electrical characteristics, parameter extraction, characterization methods for rigid and flexible devices, electrical stability, printed transistors; organic/polymer, metal-oxide, electrolyte gated	**9**
4	Other Flexible Devices and System Integration: Organic Light Emitting Diodes, Organic Solar Cells, thin flexible OLED displays, OLED lighting, smart wallpaper, sensors, logic, and memory, RFID tags, Latest applications of printed electronics, Encapsulation, Roll to roll printing processes, Integration Issues, and Designs for the Future.	**9**

Course Assessment Method
(CIE: 40 marks,ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	**Assignment/ Microproject**	**Internal Examination-1 (Written)**	**Internal Examination-2 (Written)**	**Total**
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Familiarize the flexible and printed electronics technology	**K2**
CO2	Understand the materials, processing and manufacturing methods for flexible devices	**K2**
CO3	Analyse the flexible thin film transistor's device structure and characterization	**K4**
CO4	To understand the latest applications of fexible printable devices	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2									
CO2	3	3	2									
CO3	3	3	2									
CO4	3	3	2									

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Organic and Printed Electronics: Fundamentals and Applications	G. Nisato, D. Lupo, S. Ganz	CRC Press	2016
2	Handbook of Flexible and Stretchable Electronics	M. M. Hussain and N. El-Atab	CRC Press	2020
3	3D Bioprinting Revolution	Sabrie Soloman	Khanna Publishing house	2020

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Large Area and Flexible Electronics	Mario Caironi & Yong-Young Noh	WILEY-VCH	2015
2	Flexible electronics: materials and applications	Wong, William S., and Alberto Salleo	Springer	2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/YoslM2Sxihs?si=02yozFsifxWfsYQH
2	https://youtu.be/YoslM2Sxihs?si=HD8mG5nR9XuUMUgB
3	https://youtu.be/KtKG_rIPbVs?si=xuOHyOLjNQCfzNm5
4	https://youtu.be/MC1zGEmrELA?si=erqi_zobzrhiMf3D

SEMESTER S7

POWER-EFFICIENT VLSI ENGINEERING

Course Code	**PEEVT 745**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	5/3	**Exam Hours**	2 Hrs.30 Min.
Prerequisites (if any)	PCECT302 Solid State Devices	**Course Type**	5 Credit Elective

Course Objectives:

1. To equip students with a comprehensive understanding of power dissipation mechanisms in MOSFET devices, the necessity for low-power circuit design, the challenges associated with deep submicron transistor design, and the exploration of emerging low-power technologies
2. To enable students to analyse the various sources of power dissipation in digital ICs, including dynamic, short circuit, switching, glitching, and static power, and to understand the impact of design parameters on power efficiency.
3. To provide students with an in-depth understanding of low-power design approaches, including supply voltage scaling, architectural techniques, and advanced methods for reducing leakage power and improving clock distribution efficiency.
4. To equip students with the knowledge of various low-power circuit design styles, including non-clocked and clocked approaches, adiabatic switching, and energy recovery techniques, to minimize power consumption in VLSI circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Physics of Power dissipation in MOSFET devices** Need for low power circuit design, MIS Structure **Deep submicron transistor design issues: Short channel effects** Channel Length Modulation , Surface scattering, Punch through, Velocity	9

	saturation, Impact ionization, Hot electron effects, Body Effect, Narrow width effect, V_{th} roll-off, Drain Induced Barrier Lowering, Gate Induced drain leakage, Tunneling Through Gate Oxide, Subthreshold Leakage Current, **Emerging Technologies for Low Power:** Hi-K Gate Dielectric, Lightly Doped Drain–Source, Silicon on Insulator	
2	**Sources of power dissipation in digital ICs** – **Dynamic Power Dissipation:** Short Circuit Power: Short Circuit Current of Inverter , Short circuit current dependency on input rise and fall time, Variation of shortcircuit current with load capacitance. Switching power dissipation: Switching Power of CMOS Inverter, Switching activity and its effects. Glitching Power: Glitches and its effect on power dissipation **Static Power Dissipation:** Sources of Leakage Power, Effects of V_{dd} and V_t on speed, Constraints on V_t Reduction.	9
3	**Low-Power Design Approaches-** **Supply Voltage Scaling for Low Power:** Effect of Supply voltage on Delay and Power Effect of Supply voltage on Static and Dynamic Power Multi VDD ,Dynamic VDD, Dynamic Voltage and Frequency Scaling (DVFS) Approaches. Architectural Level Approaches: Pipelining and Parallel Processing **Leakage power reduction Techniques:** Effect of threshold voltage on Leakage Power Transistor stacking, MTCMOS, VTCMOS Power gating& Clock gating Techniques. Power-Efficient Clock Distribution	9

4	**Circuit Design Styles for Low Power-** **Non clocked circuit design style:** Fully Complementary logic. NMOS and Pseudo –NMOS logic, Differential Cascode Voltage Switch logic(DCVS) **Clocked design style:** Basic concept, Dynamic Logic, Domino logic, Differential Current Switch Logic. **Adiabatic switching** – Adiabatic charging, Adiabatic amplification, Adiabatic logic gates, Pulsed power supplies. Energy Recovery Circuit Techniques	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Internal Ex	Evaluate	Analyse	Total
5	**15**	**10**	**10**	**40**

Criteria for Evaluation (Evaluate and Analyse): 20 marks

1. Literature Review and Report (10 Marks)

Assessment Method:

- Students select recent publications on a specific topic related to the course (eg. Hi-K Gate Dielectrics).
- Preparation of a report summarizing the findings, discussing the significance, and proposing future research directions.

Criteria:

- Relevance of Chosen Publications (2 Marks): Selection of up-to-date and significant research papers.
- Depth of Analysis (4 Marks): Thorough understanding and critical analysis of the literature.
- Clarity and Organization (2 Marks): Well-structured report with clear arguments.
- Originality (2 Marks): Innovative insights or perspectives.

2. Design Exercise (5 Marks)

Assessment Method:

- Design a basic adiabatic logic gate (e.g., AND, OR, XOR) using a simulation tool such as Cadence or HSPICE, simulate the circuit, analyze the power consumption, and compare it with a conventional CMOS logic gate.
- Preparation of a detailed report.

Criteria for Assessment (Total: 5 Marks):

- **Correctness of the Design (2 Marks)**:
  - The logic gate must function correctly, with accurate simulation results that match the expected logical behavior.
- **Power Consumption Analysis (2 Marks)**:
  - Students should provide a comparative analysis showing how the adiabatic logic gate consumes less power compared to a traditional CMOS gate. This should include quantitative data from the simulation.
- **Clarity and Completeness of the Report (1 Mark)**:
  - A concise report detailing the design process, simulation setup, results, and conclusions. The report should be well-organized and clear, making it easy to follow the student's work.

4. Case Study Analysis (5 Marks)

Assessment Method:

Task: Students will be given a case study that involves a complex CMOS circuit. They will be required to identify and analyze the sources of switching power dissipation within the circuit, propose optimization techniques, and predict the potential power savings.

Criteria for Assessment (Total: 5 Marks):

- **Identification of Switching Power Sources (2 Marks)**:
  - Accurate identification of all key areas within the CMOS circuit where switching power dissipation occurs.
- **Proposed Optimization Techniques (2 Marks)**:
  - Thoughtful and feasible suggestions for minimizing switching power dissipation, including explanations of how these techniques would work in the given circuit.
- **Predicted Power Savings and Justification (1 Mark)**:
  - A reasoned estimation of the potential power savings from the proposed optimizations, supported by logical arguments or simple calculations.

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. Each question carries 9 marks. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Analyse and evaluate power dissipation mechanisms in MOSFET devices, understand the need for low-power design, identify deep submicron transistor design challenges, and apply emerging technologies to optimize power efficiency in VLSI circuits.	**K3**
CO2	Identify and quantify various sources of power dissipation in digital ICs, including dynamic, short circuit, switching, glitching, and static power, and evaluate strategies for optimizing power consumption.	**K2**
CO3	Apply various low-power design approaches, including supply voltage scaling, architectural optimizations, and leakage power reduction techniques, to enhance power efficiency in VLSI circuits.	**K3**
CO4	Design and evaluate low-power circuits using various design styles, including non-clocked and clocked approaches, adiabatic switching, and energy recovery techniques, to effectively reduce power consumption in VLSI systems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**3**		**1**				**1**	**1**		
CO2	**3**	**2**	**2**	**2**	**1**				**1**	**1**		
CO3	**3**	**3**	**3**		**2**				**1**	**1**		
CO4	**3**	**2**	**3**	**2**	**2**				**1**	**1**		

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design of Analog CMOS Integrated Circuits	Behzad Razavi	McGraw-Hill	2/e, 2002
2	CMOS: Circuits Design, Layout and Simulation,	Baker, Li, Boyce,	Prentice Hall India,	1994
3	Microelectronic Circuits	Sedra & Smith	Oxford University Press	6/e,2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design,	Phillip E. Allen, Douglas R. Holbery	Oxford University Press	3/e
2	Fundamentals of Microelectronics	Behzad Razavi	Wiley student Edition	2014
3	Analysis and Design of Analog Integrated Circuits	Meyer Gray , Hurst, Lewis	Wiley	5/e, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
2	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
3	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
4	Switching Circuits and Logic Design by Prof. Indranil Sengupta Lectures 47-51

SEMESTER 7

RF MICROELECTRONICS

Course Code	PEEVT 751	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

This Course aims

1. To provide an overview of passive components and lumped elements circuits.
2. To understand the fabrication of microwave integrated circuits.
3. To study various planar transmission lines.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Passive Components, Inductors- printed inductors, wire inductors, resistors, capacitors, Monolithic capacitors, Via –holes and grounding. (No detailed analysis required). Lumped element circuits: Passive Circuits-filters and Couplers, Power dividers/ Combiners, Lumped Elements for biasing circuit, Phase Shifters, Digital Attenuators. (No detailed analysis required)	9
2	Microwave integrated circuit fabrication technology Introduction - Materials, Mask layout, Mask fabrication, Printed Circuit Boards- PCB Fabrication, PCB Inductors. Microwave Printed Circuits - MPC fabrication.	9

3	Hybrid integrated circuits Thin Film Technology, Thick film Technology- Coirfed Ceramic and Glass ceramic Technology. MMIC Fabrication, Steps Involved in the Fabrication of MOSFET, CMOS Fabrication, Micromachining fabrication.	**9**
4	Microstrip overview Introduction to Planar Transmission Line, Various types of planar transmission lines. Microstrip Lines, Introduction to Slot line and Coupled lines.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Discuss about the RF components and circuits.	**K2**
CO2	Explain about PCB fabrication.	**K2**
CO3	Understand MMIC Technology	**K2**
CO4	Explain about Microstrip Lines	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**										**2**
CO2	**3**	**2**										**2**
CO3	**3**	**2**										**2**
CO4	**3**	**2**										**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Radio Frequency Integrated Circuits and Technologies	Frank Ellinger	Springer	2007
2	Lumped Elements for RF and Microwave Circuits	Inder Bahl	Artech House	2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	RF Microelectronics	B.Razavi	Prentice-Hall PTR	1998
2	Microwave Integrated Circuits	Gupta K. C. &Amarjit Singh	John Wiley & Sons	1975
3	RFIC and MMIC Design and Technology	I.D Robertson,C .Lucyszyn	The Institution of Engineering and Technology	2001
4	Passive RF & Microwave Integrated Circuits	Leo G. Maloratsky	Elsevier	2004

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/cHbcdk-C4Zo?si=MAMALiV4ffGdQOAO
2	https://youtu.be/pgcqahZEdpY
3	https://youtu.be/lW0QMvmeVGs?si=lTNG13H6s1Jy-_Ip
4	https://youtu.be/ap9739K_OJo

SEMESTER S7

INTERNET OF THINGS

Course Code	PEECT 752	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. This course aims to introduce IoT fundamentals.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to IoT technology:** Definitions of IoT, Characteristics of IoT devices – power, computational constraints, IoT Architectural view – Middleware based architecture, Service oriented architecture, M2M Communication and IoT, Typical application areas of IoT technology (case studies of at least four domains) - Energy management and Smart grid, IoT for Home, Cities, Environment monitoring, Agriculture, Supply chain and customer monitoring	9
2	**Components of IoT technology:** Identification/Addressing - Electronic Product Codes, RFID, ubiquitous code, IPv4, IPv6. Sensors and Actuators*. IoT Hardware**, IoT Software – overview of Operating systems, Firmware, Middle ware, Application software used in IoT. Connectivity for IoT devices – characteristics.	9
3	**Communication technologies for IoT :** Zigbee - key features, architecture, limitations, Bluetooth technology - bluetooth stack, piconet, scatternet, limitations, Bluetooth Low Energy (key features, architecture, limitations), Wifi (IEEE 802.11) technology – key features, limitations, Cellular technology – GSM, 3G, 4GLTE (overview), features, limitations, LoRa technology – features, LoRaWAN architecture, 6LoWPAN – features, protocol stack, Narrow Band (NB- IoT) – features, applications, Sigfox – features, applications	9

4	**IoT Data Management :** Storage technologies for IoT hardware – Volatile, Non-volatile, Embedded (MTP/OTP), external flash (NAND/NOR), DRAM, eflash, UFS, eMMC (overview of technologies). Cloud and IoT, Cloud computing – architecture, advantages of cloud computing, Software as a Service (SaaS), Platform as a Service (PaaS), Infrastructure as a Service (IaaS). Case study of commercial cloud computing platforms like - Microsoft Azure IoT Suite, Google Cloud's IoT Platform, IBM Watson IoT Platform. IoT analytics	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain in a concise manner the architecture of IoT	**K2**
CO2	Identify various hardware and software components used in IoT	**K3**
CO3	Discuss the various communication technologies and interfaces in IoT	**K2**
CO4	Describe the usage of modern technologies like cloud computing for data management in IoT	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	2	2								2
CO2	3	2	2	2								2
CO3	3	2	2	1								2
CO4	3	2	2	1								2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Internet of Things : Architecture and Design Principles"	Rajkamal	McGraw Hill (India) Private Limited.	2nd edition,2022
2	"Internet of Things (A Hands-on-Approach)"	Vijay Madisetti and Arshdeep Bahga	Orient Blackswan Private Limited - New Delhi	1st Edition,2015

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Internet of things: A survey on enabling technologies, protocols, and applications	Al-Fuqaha	IEEE Communications Surveys & Tutorials	2015
2	The Internet of Things	Samuel Greengard	The MIT Press Essential Knowledge series Paperback	March 20, 2015
3	The Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems	Ovidu Vermesan and Peter Friess	River Publishers	1st Edition, 2013
4	. Internet of Things - From Research and Innovation to Market Deployment	Peter Friess, Ovidiu Vermesan	River Publishers	1st Edition,2014

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/WUYAjxnwjU4?si=s58W-NKMrEQMaJ8m https://youtu.be/BXDxYh1EV2w?si=8oFtQB9vycC_c-t2
2	https://youtu.be/z3VEZPwl5gA?si=tNuzG_By-KBU3ks_ https://youtu.be/SXz0XR68dwE?si=1tVN1g9FQcGp87li https://youtu.be/TvzgzO6xKrY?si=gYzJstW51MTNsgKj
3	https://youtu.be/qko-f1VDhCM?si=0tWM_OHS395ESV_w https://youtu.be/d9QfVpCG00Y?si=qeHk8tPg_torr2yX https://youtu.be/1zQ8wbBozqI?si=7vOSHMt8OT3nQINO
4	https://youtube.com/playlist?list=PLE7VH8RC_N3bpVn-e8QzOAHziEgmjQ2qE&si=rr5Fpuew5q9_Y4qg

SEMESTER S7

ELECTROMAGNETIC COMPATIBILITY AND SIGNAL INTEGRITY

Course Code	PEEVT753	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To provide an understanding of important concepts of Electromagnetic Compatibility which are fundamentalfor the design of electronics systems and devices in order to minimize electromagnetic interference.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to Aspects of EMC**: EMI Sources, EMC units, Signalsource specification, Advantages of EMC Design, EMC Requirementsfor Electronic Systems, Measurement of Radiated and Conducted Emissions.	8
2	**Signal Integrity:** Transmission-Line Equations, High-Speed Digital Interconnects,Effect of Terminations, Matching Schemes, Effects of LineDiscontinuities. Non-ideal Behaviour of Components: Wires, resistors,capacitors, inductors, Printed Circuit Board (PCB), Effect of Component, Leads, Mechanical Switches	10
3	**Conducted Emissions and Conducted Susceptibility**: Measurement,Power Supplies, Filters, Placement. Radiated Emissions andConducted Susceptibility: Simple Emission Models for Wires and PCBLands, Simple Susceptibility Models for Wires and PCB Lands	8
4	**Crosstalk:** Three-Conductor Transmission Lines and Crosstalk, ShieldedWires, Twisted Wires. **Shielding**: Shielding Effectiveness- Far-FieldSources, Near-Field Sources; Low Frequency, Magnetic Field Shielding **System Design for EMC:**Common EMC Issues in Practice and Design Guidelines	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Implement the various measurement techniques for electromagnetic interference and for electromagnetic compatibility	**K3**
CO2	Recognize the various agencies and standards associated with EMI/EMC	**K2**
CO3	Analyse various EM compatibility issues with regard to the design of PCBs and ways to improve the overall system performance	**K4**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**2**							**3**		**3**
CO2	**3**	**3**	**2**							**3**		**2**
CO3	**3**	**3**	**3**							**3**	**3**	**3**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introductionto Electromagnetic Compatibility	C. R. Paul	John Wiley & Sons	3rd Edition,2022
2	Electromagnetic Compatibility Engineering	H. W. Ott	John Wiley & Sons	2nd Edition, 2009
3	Engineering EMC Principles, Measurementsand Technologies,	V. P. Kodali	Wiley-Blackwell	2nd Edition, 2001

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Electromagnetic Compatibility in Medical Equipment	W. D. Kimmel and D. Gerke	IEEE&Interpharm Press	1995

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/108/106/108106138/
2	https://onlinecourses.nptel.ac.in/noc24_ee67/preview
3	https://archive.nptel.ac.in/content/syllabus_pdf/108106138.pdf
4	https://www.digimat.in/nptel/courses/video/108106138/L28.html

SEMESTER S7

INFORMATION THEORY & CODING

Course Code	**PEEVT754**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Linear Algebra and Calculus, Probability, Random Process and Numerical Methods, Signals and Systems.	**Course Type**	Theory

Course Objectives:

1. To lay down the foundation of information theory introducing both source coding and channel coding
2. To expose students to algebraic and probabilistic error-control codes that are used for reliable transmission

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Entropy, Properties of Entropy, Joint and Conditional Entropy, Mutual Information, Properties of Mutual Information. Discrete memoryless sources, Source code, Average length of source code, Bounds on average length, Uniquely decodable and prefix-free source codes. Kraft Inequality (with proof), Huffman code. Shannon's source coding theorem (both achievability and converse) and operational meaning of entropy.	**9**
2	Discrete memoryless channels. Capacity of discrete memoryless channels. Binary symmetric channels (BSC), Binary Erasure channels (BEC). Capacity of BSC and BEC. Channel code. Rate of channel code. Shannon's channel coding theorem (both achievability and converse without proof) and operational meaning of channel capacity. Modeling of Additive White Gaussian channels. Continuous-input channels with average power constraint. Differential entropy. Differential Entropy of Gaussian random variable. Relation between differential entropy and entropy. Shannon-Hartley theorem (with proof – mathematical subtlities	**9**

	regarding power constraint may be overlooked). Inferences from Shannon Hartley theorem – spectral efficiency versus SNR per bit, power-limited and bandwidth-limited regions, Shannon limit, Ultimate Shannon limit.	
3	Overview of Groups, Rings, Finite Fields, Construction of Finite Fields from Polynomial rings, Vector spaces. Block codes and parameters. Error detecting and correcting capability. Linear block codes. Two simple examples -- Repetition code and single parity-check code. Generator and parity-check matrix. Systematic form. Maximum likelihood decoding of linear block codes. Bounded distance decoding. Syndrome. Standard array decoding.	**9**
4	Cyclic codes. Polynomial and matrix description. Interrelation between polynomial and matrix view point. Systematic encoding. Decoding of cyclic codes. (Only description, no decoding algorithms) Hamming Codes, BCH codes, Reed-Solomon Codes Convolutional Codes. State diagram. Trellis diagram. Maximum likelihood decoding. Viterbi algorithm. Low-density parity check (LDPC) codes. Tanner graph representation. Message-passing decoding for transmission over binary erasure channel.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain measures of information – entropy, conditional entropy, mutual information	**K2**
CO2	Apply Shannon's source coding theorem and channel capacity for data compression.	**K3**
CO3	Apply linear block codes for error detection and correction	**K3**
CO4	Apply algebraic codes with reduced structural complexity for error correction	**K3**
CO5	Understand encoding and decoding of convolutional and LDPC codes	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3										
CO2	3	3	2	3	3							
CO3	3	3	2	3	3	2						2
CO4	3	3	2	3	3	2						2
CO5	3	3	2	3	3	2						2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Elements of Information Theory.	Joy A Thomas, Thomas M Cover,	Wiley-Interscience	1st
2	Digital Communication Sysmtes	Simon Haykin,	Wiley.	2nd
3	Principles of digital communication	RG Gallager	Cambridge University Press	2010
4	Information Theory, Inference and Learning Algorithms", ,	David JC McKay	Cambridge University Press	1st

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Modern Coding Theory	Rüdiger Urbanke and TJ Richardson	Cambdridge University Press	1st
2	Error Control Coding: Fundamentals and Applications,	Shu Lin & Daniel J. Costello. Jr.,	Wiley	2nd Edition.
3	Introduction to Coding Theory	Ron M Roth	Cambrdige University Press	1st

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117101053
2	https://nptel.ac.in/courses/117108097
3	https://archive.nptel.ac.in/noc/courses/noc18/SEM2/noc18-ee39/
4	https://archive.nptel.ac.in/courses/117/104/117104120/

SEMESTER S7

OPTOELECTRONIC DEVICES

Course Code	PEEVT 756	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To provide an insight over the working principles and performance parameters of various optoelectronics devices used for optical networks and communication

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Fundamentals of Semiconductor Optoelectronics** Optical processes in semiconductors: electron-hole generation and recombination, Absorption, Auger recombination, Heat generation and dissipation, Heat sources.Various light production mechanisms,Indirect band gap materials, Semiconductors used for optical Applications, Basic principle of LED and LASER, Spontaneous emission and Stimulated Emission, Coherence of sources.	9
2	**Optical Sources** Construction and Operation of LEDs, Heterojunctios, Surface Emitter and Edge Emitter LEDs, Characteristics of LEDs, LASERs, Threshold Condition for lasing, Line Broadening Mechanisms, Fabry-Perot Lasers, Distributed Feedback(DFB) Lasers, Distributed Bragg Reflector(DBR) Lasers, Vertical Cavity Surface Emitting Lasers (VCSELs), In-Fibre Lasers.	9

3	**Optical Detectors** Principle of Photo Detection,Working of LDR, PN diode, PIN diode, Avalanche Photodiode (APD), Characteristics of APD, Resonant Cavity Photo detector, Photo Transistor, Quantum efficiency, Responsivity, Noise in Photo detectors, Thermal Noise, Dark Current, Shot Noise, Quantum limit of Optical Detection.	**9**
4	**Optoelectronic Devices and Modulator** Optoelectronic ICs, Advantages, Liquid Crystal Display, Structure, TFT display, Structure, Polymer LED, Organic LED, Optical Modulators using PN junction, Electro-Optic Modulators, Acousto-Optic Modulators, Raman-Nath Modulators, Optical switching and Logic devices,Optical Memory. Solar Cells: basic working principle, VI Characteristics, Different types of solar cells, Dye sensitized solar cells (DSSC), Perovskite Solar cells.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand physics of optical processes in semiconductors.	**K2**
CO2	Distinguish different optical sources used in optoelectronic applications.	**K3**
CO3	Analyse different types of photo detectors based on their performance parameters	**K3**
CO4	Explain various optical modulators and optoelectronic devices.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**											**2**
CO2	**3**											**2**
CO3	**3**		**2**		**2**							**2**
CO4	**3**		**2**		**2**							**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of Light Sources and Lasers	Mark Csele,	Wiley-Interscience,	2004
2	Solid State Lasers	W.Koechner,M.Bass	Springer,	2003
3	Photonics Optical Electronics in modern communication	Yariv,	Oxford University Press,	6/e , 2006.
4	Understanding Optical Communications,	Harry J R Dutton	IBM	1/e 1998

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Organic Light-Emitting Diodes,	Alastair Buckley	Woodhead,	2013 6,
2	Solar Cell Device Physics	Stephen J Fonash	Elsevier	2/e, 2010

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/113/104/113104012/
2	https://archive.nptel.ac.in/courses/115/102/115102026/
3	https://www.youtube.com/watch?v=WWjldCmRteg
4	https://archive.nptel.ac.in/courses/113/106/113106065/

SEMESTER S7

VLSI ARCHITECTURES FOR DSP

Course Code	PEEVT 757	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	VLSI	Course Type	Theory

Course Objectives:

1. Equip students with the ability to represent DSP algorithm Representations and Techniques
2. Develop student's proficiency in designing and implementing pipelined and parallel processing structures for DSP applications
3. Enable students to apply retiming and transformation techniques:
4. Train students to analyze and compute scaling and round-off noise in digital filters.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Representations of DSP algorithms - Block Diagram, Signal Flow Graph, Data Flow Graph, Dependence Graph. Loop Bound & Iteration Bound, Definition, Examples, Algorithms for Computing Iteration Bound – Longest Path Matrix Algorithm, Minimum Cycle Mean Algorithm, Iteration Bound of Multirate Data-Flow Graphs.	9
2	Pipelining and Parallel Processing - Pipelining of FIR Digital Filters, Data-Broadcast Structures, Fine-Grain Pipelining. Parallel Processing, Pipelining, and Parallel Processing for Low Power. Retiming: Definition and Properties, Solving System of Inequalities, Retiming Techniques- Cutset Retiming and Pipelining, Retiming for Clock Period Minimization, Retiming for Register Minimization	9

3	Unfolding: Properties of Unfolding, Critical Path, Unfolding and Retiming, Application of Unfolding, Sample Period Reduction, Parallel Processing. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.	**9**
4	Scaling and round off noise – scaling and round off noise, state variable description of digital filters, scaling and round off noise computation, round off noise in pipelined IIR filters, Round off noise omputation using state variable description, slow down, retiming and pipelining	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Represent DSP algorithms using block diagrams, signal flow graphs, data flow graphs, and dependence graphs, and analyze iteration bounds using relevant algorithms.	**K3**
CO2	Demonstrate the ability to design, implement, and optimize pipelined and parallel processing structures for DSP systems, including FIR digital filters and data broadcast structures, focusing on low-power solutions.	**K4**
CO3	Apply retiming techniques to minimize clock periods and registers and use unfolding and folding transformations to optimize DSP architectures.	**K6**
CO4	Become Proficient in evaluating and mitigating scaling and round-off noise in digital filters, particularly in pipelined IIR filters, using state variable descriptions and related computation techniques.	**K5**
CO5	Design efficient DSP architectures by integrating knowledge of algorithm representations, pipelining, parallel processing, retiming, and noise mitigation techniques.	**K6**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	**3**	**2**	**3**	**2**	**1**							
CO2	**3**	**3**	**3**	**2**	**2**	**1**						
CO3	**3**	**3**	**2**	**3**	**2**	**1**						
CO4	**2**	**3**	**2**	**3**	**1**	**1**						
CO5	**3**	**3**	**3**	**3**	**2**	**2**						

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI DSP Systems- Design and Implementation	Keshab K Parhi	John Wiley	1st Edn 1999.
2	Digital Signal processing for multimedia systems	Keshab K Parhi and Takao Nishitami	CRC press	2018
3	Digital Signal Processing with Field Programmable Gate Arrays	Uwe Meyer-Baese	Springer	4th Edn, 2014
4	VLSI Design Methodology Development	Thomas Dillinger	Prentice Hall	1st Edn 1998
5	Advanced Digital Signal Processing and Noise Reduction	Saeed V. Vaseghi	Wiley	4th Edn 2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Understanding digital signal processing	Richard G Lyons	Pearson Education India	3,1997
2	DSP Integrated Circuits	Lars Wanhammar	Academic Press	1st Edn 1999
3	Digital Filter Design	T. W. Parks and C. S. Burrus	Wiley-Interscience	1st Edn 1987
4	Architectures for Digital Signal Processing	Peter Pirsch	John Wiley & Sons	1st Edn 1998
5	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste and David Harris	Pearson	4th Edn 2010

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc20_ee44/preview
2	https://www.youtube.com/playlist?list=PLT1QAv48lhQKwFZ0TkqpJaUm2LeW9226z

SEMESTER 7

AI AND ML FOR VLSI CAD

Course Code	PEEVT 758	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Machine Learning	Course Type	Theory

Course Objectives:

1. To provide students with a comprehensive understanding of the applications of Artificial Intelligence and Machine Learning in VLSI CAD.
2. To introduce students to the concept of Compact Process Models (CPM) in lithographic patterning, enabling them to develop and train machine learning models for accurate representation and optimization of the lithographic process.
3. To equip students with the skills to apply machine learning algorithms for various aspects of physical design, mask synthesis, and physical verification in VLSI, focusing on enhancing efficiency, accuracy, and automation.
4. To train students in using machine learning techniques for yield estimation, reliability analysis, and testing in high-volume VLSI manufacturing, improving process optimization, and reliability prediction.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to AI and ML in VLSI CAD:** Overview of AI and ML applications in VLSI CAD, Unsupervised, Supervised, and Semisupervised Learning, Introduction to neural networks and decision trees **Introduction to VLSI Design Methodologies:** VLSI Design Cycle - Physical Design Cycle - Design Styles and comparison of different Design Styles, Fabrication of VLSI Circuits. **Machine Learning for Compact Lithographic Process Models:** Introduction, Lithographic Patterning Process, Representation of Lithographic Patterning Process – Mask, Imaging, Resist & Etch Transfer Function, Compact process model machine learning problem statement, CPM Task, CPM Training Experience, Performance metrics, Supervised	9

	learning of a CPM	
2	**Neural Network Compact Patterning Models:** Neural Network Mask Transfer Function, Neural Network Image Transfer Function, Neural Network Resist Transfer Function, Neural Network Etch Transfer Function **Machine Learning for Mask Synthesis** Introduction, Machine Learning guided OPC, MLP Construction, ML-EPC, EPC Algorithm **Machine Learning in Physical Verification** Introduction, Machine Learning in Physical Verification – layout feature extraction & encoding, models for hotspot detection.	**9**
3	**Machine Learning in Mask Synthesis and Physical Design**: Machine Learning in Mask Synthesis – mask synthesis flow, Machine Learning for sub-resolution assist features, Machine Learning for optical proximity correction. Machine Learning in Physical Design - for datapath placement, routability driven placement, clock optimization, lithography friendly routing **Machine Learning for Manufacturing**: Gaussian Process-Based Wafer-Level Correlation Modeling and Its Applications	**9**
4	**Machine Learning for Yield and Reliability:** High-volume manufacturing yield estimation – Histogram with random sampling, Histogram with GPST-PS, Kernel density estimation. Machine learning-based aging analysis. **Learning-Based VLSI Test and Verification:** VLSI Testing Process, Off-Chip Testing, On-Chip Testing, Combinational Circuit Testing, Sequential Circuit Testing, Advantages of VLSI Testing, Machine Learning's Advantages in VLSI Design, Ease in the Verification Process, Time-Saving, 3Ps (Power, Performance, Price), Electronic Design Automation, System-Level Design, Logic Synthesis and Physical Design, Test, Diagnosis, and Validation, Verification, Challenges	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply AI and ML concepts to VLSI CAD problems	**K3**
CO2	Develop and train machine learning models for lithographic process modeling	**K6**
CO3	Implement machine learning algorithms for physical design automation and verification	**K3**
CO4	Analyze machine learning-based solutions for yield estimation and reliability in VLSI manufacturing	**K4**
CO5	Evaluate the effectiveness of AI/ML techniques in VLSI testing and verification	**K5**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**	**1**									
CO2	**3**	**2**	**2**	**1**							**1**	
CO3	**3**	**2**	**1**	**1**							**1**	
CO4	**3**	**2**	**1**	**2**								**1**
CO5	**3**	**2**	**1**	**2**								**1**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Joobbani, R. An Artificial Intelligence Approach to VLSI Routing.	Joobbani, R.	Springer Science & Business Media	2012
2	VLSI Physical Design Automation.	Sait, Sadiq.	World Scientific,	1999
3	Machine Learning in VLSI Computer-Aided Design.	Elfadel, Ibrahim.	Springer,	2019
4	VLSI Physical Design: From Graph Partitioning to Timing Closure.	Kahng, Andrew.	Springer Nature	2022
5	Machine Learning Applications in Electronic Design Automation.	Ren, Haoxing.	Springer Nature	2023

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Layout Optimization in VLSI Design.	Lu, Bing.	Springer Science & Business Media	2001
2	Machine Learning for VLSI Chip Design	Abhishek Kumar, Suman Lata Tripathi and K Srinivasa Rao	John Wiley & Sons	2023

SEMESTER S7

ADVANCED VLSI ARCHITECTURES FOR DSP

Course Code	PEEVT 755	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	ESE Marks	60
Credits	5/3	Exam Hours	2Hrs.30 Min.
Prerequisites (if any)	VLSI		

Course Objectives:

1. Equip students with the knowledge of pipelining and parallel processing techniques
2. Enable students to comprehend and apply retiming and unfolding techniques for system optimization.
3. Develop the ability to implement and analyze fast convolution algorithms and advanced filtering methods.
4. Train students to design and optimize bit-level arithmetic architectures, focusing on efficiency and noise reduction.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Pipelining and Parallel Processing - Pipelining of FIR Digital Filters, Data-Broadcast Structures, Fine-Grain Pipelining. Parallel Processing, Pipelining, and Parallel Processing for Low Power. Retiming: Definition and Properties, Solving System of Inequalities, Retiming Techniques- Cutset Retiming and Pipelining, Retiming for Clock Period Minimization, Retiming for Register Minimization	9
2	Unfolding: Properties of Unfolding, Critical Path, Unfolding and Retiming, Application of Unfolding, Sample Period Reduction, Parallel Processing. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.	9
3	Fast convolution – Cook Toom Algorithm, Winograd Algorithm, Iterated convolution, Cyclic convolution	9

	Algorithmic strength reduction in filters and transforms- Parallel FIR filters, DCT and IDCT, Pipelined and parallel recursive and adaptive filters- pipeline interleaving in Digital filters, Pipelining in IIR digital filters, Parallel processing for IIR filters, Low power IIR filter design using pipelining and parallel processing.	
4	Digital lattice filter structures- Schur algorithm, Digital basic lattice filters, Derivation of one multiplier Lattice filter, Derivation of scaled-normalized lattice filter, Round off noise calculation in Lattice filters. Bit level arithmetic architectures- parallel multipliers, interleaved floor plan and bit plane based digital filters, bit serial filter design and implementation, Canonic signed digital arithmetic.	**9**

Criteria for Evaluation (Evaluate and Analyse): 20 marks

Evaluation Methods:

1: Practical Experiments Using Design and Analysis Tools (10 marks)

Students will perform specific experiments using tools like MATLAB/Simulink, Cadence Virtuoso, Xilinx Vivado Design Suite, or Synopsys Design Compiler. Each experiment will focus on implementing and analyzing different DSP architectures and techniques.

2: Course Project (10 marks)

Comprehensive project involving design, implementation, and analysis of different DSP architectures models. Project phases: Proposal, Design, Implementation, Testing, Final Report, Presentation, and Viva Voce.

Sample Experiments:

Experiment 1: Design and simulate a pipelined FIR filter.

- ***Objective:*** Understand the impact of pipelining on the performance and power consumption of FIR filters.
- ***Tools Used:*** MATLAB/Simulink
- ***Steps Involved:***
    - Define the FIR filter specifications (filter order, cutoff frequency).

- Design the FIR filter using MATLAB.
- Implement the filter in Simulink and add pipelining stages.
- Simulate the filter and compare performance metrics (latency, power consumption) with and without pipelining.
- Analyze and document the results.

Experiment 2: Design an unfolded DSP system to reduce the critical path.

- ***Objective:*** Learn how unfolding can reduce the critical path and enhance system throughput.
- ***Tools Used:*** MATLAB/Simulink
- ***Steps Involved:***
  - Select a DSP algorithm (e.g., FIR filter).
  - Implement the algorithm in MATLAB.
  - Apply unfolding techniques to the algorithm.
  - Simulate the original and unfolded designs in Simulink.
  - Compare critical paths and document the performance improvements.

Experiment 3: Design and simulate the Winograd convolution algorithm.

- ***Objective:*** Demonstrate the computational benefits of the Winograd algorithm over conventional methods.
- ***Tools Used:*** Xilinx Vivado
- ***Steps Involved:***
  - Study the Winograd algorithm theory.
  - Implement the algorithm in HDL.
  - Simulate the design in Vivado.
  - Compare the computational efficiency with conventional convolution methods.
  - Document the findings.

Experiment 4: Implement a scaled-normalized lattice filter and analyze noise reduction techniques.

- ***Objective:*** Evaluate round-off noise reduction in digital lattice filters.
- ***Tools Used:*** Cadence Virtuoso
- ***Steps Involved:***
  - Design a lattice filter in HDL.
  - Implement the design in Cadence Virtuoso.
  - Apply scaled-normalized techniques for noise reduction.
  - Simulate the filter and analyze round-off noise.
  - Document the noise reduction results.

Sample Project Topics:

1. Design a low-power parallel processing architecture for a DSP application
2. Apply retiming to minimize the clock period of a digital circuit
3. Optimize the register usage in digital circuits through retiming.
4. Apply unfolding techniques to reduce the sample period of a digital filter.
5. Implement a folded architecture for a multirate system focusing on register minimization.
6. Apply folding transformations and understand their impact on hardware resource optimization
7. Analyze the efficiency of the Cook-Toom algorithm compared to standard convolution methods
8. Design and implement a parallel FIR filter using algorithmic strength reduction techniques.
9. Implement a pipelined recursive filter using algorithmic strength reduction.
10. Design and simulate a digital lattice filter with one multiplier.
11. Design and implement a parallel multiplier architecture and evaluate their performance and efficiency.
12. Implement a bit-serial filter design for understanding the trade-offs between hardware complexity and performance in bit-serial designs.

Criteria for Evaluation: Lab Experiments (10 marks)

Understanding of Concepts (3 marks)

- Demonstrates a thorough understanding of the theoretical concepts related to the experiments.
- Correctly explains the purpose and expected outcomes.

Implementation and Accuracy (3 marks)

- Correctly implements the DSP architectures using appropriate tools.
- Ensures the design functions as expected with minimal errors.

Analysis and Problem-Solving (2 marks)

- Effectively analyzes the model performance and identifies issues.
- Demonstrates problem-solving skills in addressing challenges encountered during experiments.

Documentation and Reporting (1 mark)

- Provides detailed documentation of the experimental setup, process, and outcomes.
- Includes visualizations, code snippets, and analysis of results.

Presentation and Communication (1 mark)

- Clearly presents the experiments and their results.
- Able to answer questions and explain design choices.

Course Project (10 marks)

Project Proposal and Planning (2 marks)

- Submits a well-defined project proposal outlining objectives, methodology, and expected outcomes.
- Demonstrates thorough planning and a clear timeline for the project.

Design and Implementation (3 marks)

- Implements the project design accurately using appropriate tools and techniques.
- The design is functional and meets the project objectives.

Innovation and Creativity (2 marks)

- Introduces innovative ideas or unique approaches in the design and implementation.
- Demonstrates creativity in solving problems or optimizing designs.

Analysis and Testing (2 marks)

- Effectively analyzes the project design to identify and address any issues.
- Conducts thorough testing to verify the functionality and performance of the model.

Final Report and Presentation (1 mark)

- Submits a comprehensive final report detailing the project, including objectives, design, methodology, analysis, and results.
- Clearly presents the project and its outcomes, and effectively communicates the key points.

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. Each question carries 9 marks. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Demonstrate an understanding of pipelining and parallel processing techniques in DSP systems, including the design and implementation of pipelined FIR digital filters and low power parallel processing architectures.	**K3**
CO2	Apply retiming techniques to optimize digital circuits for clock period and register minimization, solving system inequalities and implementing cutset retiming and pipelining.	**K5**
CO3	Utilize unfolding and folding transformations to reduce critical path and register usage in DSP architectures, and apply these techniques to multirate systems for sample period reduction.	**K4**
CO4	Implement advanced convolution algorithms such as Cook-Toom and Winograd, and apply algorithmic strength reduction techniques to enhance the performance of FIR and IIR filters	**K6**
CO5	Design and analyze digital lattice filter structures and bit-level arithmetic architectures, including parallel multipliers, bit-plane-based digital filters, and bit-serial filter designs, focusing on performance optimization and noise reduction.	**K6**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**2**		**3**							
CO2	**3**	**3**	**2**		**3**							
CO3	**3**	**3**	**2**		**3**							
CO4	**3**	**3**	**2**		**3**							
CO5	**3**	**3**	**2**		**3**							

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI DSP Systems- Design and Implementation	Keshab K Parhi	John Wiley	1st Edn 1999.
2	Digital Signal processing for multimedia systems	Keshab K Parhi and Takao Nishitami	CRC press	2018
3	Digital Signal Processing with Field Programmable Gate Arrays	Uwe Meyer-Baese	Springer	4th Edn, 2014
4	VLSI Design Methodology Development	Thomas Dillinger	Prentice Hall	1st Edn 1998
5	Advanced Digital Signal Processing and Noise Reduction	Saeed V. Vaseghi	Wiley	4th Edn 2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Understanding digital signal processing	Richard G Lyons	Pearson Education India	3,1997
2	DSP Integrated Circuits	Lars Wanhammar	Academic Press	1st Edn 1999
3	Digital Filter Design	T. W. Parks and C. S. Burrus	Wiley-Interscience	1st Edn 1987
4	Architectures for Digital Signal Processing	Peter Pirsch	John Wiley & Sons	1st Edn 1998
5	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste and David Harris	Pearson	4th Edn 2010

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc20_ee44/preview
2	https://www.youtube.com/playlist?list=PLT1QAv48lhQKwFZ0TkqpJaUm2LeW9226z

SEMESTER S7

MECHATRONICS

Course Code	OEEVT 721	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To provide knowledge about the integration of mechanical, electronics, control and computer engineering in the design of mechatronics systems.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Mechatronics: Structure of Mechatronics system. Sensors - Characteristics - Temperature, flow, pressure sensors. Displacement, position and proximity sensing by magnetic, optical, ultrasonic, inductive, capacitive and eddy current methods. Encoders: incremental and absolute, gray coded encoder. Resolvers and synchros. Piezoelectric sensors. Acoustic Emission sensors. Principle and types of vibration sensors. Actuators: Mechanical actuators, Electrical actuators, Hydraulic and Pneumatic actuators Directional control valves, pressure control valves, process control valves. Rotary actuators. Development of simple hydraulic and pneumatic circuits using standard Symbols.	9
2	Mechatronics in Computer Numerical Control (CNC) machines: Design of modern CNC machines - Mechatronics elements - Machine structure: guide ways, drives. Bearings: anti- friction bearings, hydrostatic bearing and hydrodynamic bearing. Re-circulating ball screws, pre-loading methods. Re-circulating roller screws. Measuring system for NC machines - direct and indirect measuring system.	9

	System modeling - Mathematical models and basic building blocks of general mechanical, electrical, fluid and thermal systems	
3	Typical elements of open and closed loop control systems. Adaptive controllers for machine tools. Programmable Logic Controllers (PLC) –Basic structure, input/ output processing. Programming: Timers, Internal Relays, Counters and Shift registers. Development of simple ladder programs for specific purposes. Case studies of Mechatronics systems: Automatic camera, bar code reader, pick and place robot, automatic car park barrier system, automobile engine management system.	**9**
4	Mechatronics in Robotics-Electrical drives: DC, AC, brushless, servo and stepper motors. Harmonic drive. Force and tactile sensors. Range finders: ultrasonic and light-based range finders Robotic vision system - Image acquisition: Vidicon, charge coupled device (CCD) and charge injection device (CID) cameras. Image processing techniques: histogram processing: sliding, stretching, equalization and thresholding.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain the sensors and actuators used in mechatronics	**K2**
CO2	Demonstrate the various components of a CNC machine	**K2**
CO3	Explain the principles of PLCs	**K2**
CO4	Explain the robotic sensors and vision system	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**											**2**
CO2	**3**		**2**	**2**	**2**							**2**
CO3	**3**	**3**	**2**	**2**	**2**							**2**
CO4	**3**		**2**	**2**	**2**	**2**						**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Mechatronics: Electronic Control Systems in Mechanical and Electrical Engineering,	Bolton W.,	Person Education Limited, New Delhi,	2007
2	Mechatronics: Integrated Mechanical Electronic Systems,	Ramachandran K. P., G. K. Vijayaraghavan, M. S. Balasundaram,	Wiley India Pvt. Ltd., New Delhi,	2008
3	Introduction to Robotics: Analysis, Systems, Applications,.	Saeed B. Niku	Person Education, Inc., New Delhi	2006

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introduction to Mechatronics and Measurement Systems,	David G. Aldatore, Michael B. Histand	McGraw-Hill Inc., USA.	2003
2	Industrial Robotics	Gordon M. Mair	Prentice Hall International, UK,	1998
3	Mechatronics,	HMT	Tata McGraw-Hill Publishing Company Ltd., New Delhi,.	2004
4	Smart Material Systems and MEMS: Design and Development Methodologies,	Vijay K. Varadan, K. J. Vinoy, S. Gopalakrishnan,	John Wiley & Sons Ltd., England,	2006.

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc21_me27/preview
2	https://nptel.ac.in/courses/112103174
3	https://archive.nptel.ac.in/courses/112/103/112103174/
4	https://nptel.ac.in/courses/112107298

SEMESTER S7

ENTERTAINMENT ELECTRONICS

Course Code	OEEVT722	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To provide broad knowledge on various industry standards, algorithms and technologies used to carry out digital audio and video broadcasting in infotainment industry.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Review of Analog Television: Scanning, Horizontal and Vertical Synchronization, Color information, Transmission methods. NTSC and PAL standards. Digital media streaming: Packetized elementary stream of audio-video data, MPEG data stream, MPEG-2 transport stream packet, Accessing a program, scrambled programs, program synchronization. PSI, Additional (Network information and service description) information in data streams for set-top boxes.	9
2	Digital Video Broadcasting (DVB): Satellite TV broadcasting – DVB-S Parameters, DVB-S Modulator, DVB-S set-top box, DVB-S2. Cable TV broadcasting – DVB-C Standard, DVB-C Modulator, DVB- C set-top box. Terrestrial TV broadcasting – DVB-T Standard, DVB-T Modulator, DVB-T Carriers and System Parameters, DVB-T receiver.Broadcasting for Handheld devices – DVB-H Standard DVB tele-text, DVB subtitling system. Digital Audio Broadcasting (DAB): Comparison of DAB with DVB. Physical layer of DAB. DAB Modulator, DAB Data Structure, DAB single frequency networks, Data broadcastingusing DAB.	9

3	High Definition Video and Audio: Pixel resolution, Comparison with Standard Definition TV, Review of Discrete Cosine Transforms (DCT), Video Compression - Quantization levels, Horizontal/Vertical blanking interval, Vertical Color resolution, DPCM of moving pictures, DCT, Run-length coding. MPEG-4 Video coding.	9
4	Display Technology: Block diagram of video reproduction system in a TV, Cathode Ray tubes, Basic principle of Plasma displays, LC displays, Light-emitting diode displays, Field emission displays, Organic light emitting device displays. Television of future: Holographic TV, Virtual Reality, Augmented Reality.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand packetized streaming of digital media happens in the field of infotainment industry.	**K2**
CO2	Realise the critical aspects of DVB and DAB standards used for media broadcasting	**K2**
CO3	Apply video coding/compression algorithms are used to produce high-definition video in MPEG-4 standard	**K3**
CO4	Understand modern display technologies for video reproduction	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**										**2**
CO2	**3**	**3**			**2**						**2**	**2**
CO3	**3**	**3**			**3**						**2**	**2**
CO4	**3**	**3**										**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Video and Audio Broadcasting Technology: A Practical Engineering Guide (Signals and Communication Technology)	W. Fischer	Springer	2020
2	Understanding Digital Television An Introduction to DVB Systems with Satellite, Cable, Broadband and Terrestrial TV,.	Lars-Ingemar Lundström	Focal Press,Elsevier	2006
3	Newnes Guide to Televeision and Video Technology	K F Ibrahim	Newnes	2007
4	Introduction to Flat Panel Displays	Jiun-Haw Lee, David N. Liu, Shin-Tson Wu	Wiley	2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Video and HD Algorithms and Interfaces,"	C. Poynton	Morgan Kaufmann	2012.
2	Digital audio broadcasting: principles and applications of DAB, DAB+ and DMB	Wolfgang Hoeg, Thomas Lauterbach	Wiley	2009.
3	Introduction to Digital Audio	John Watkinson	Focal Press	1994.
4	Art of Digital Video,	John Watkinson	Focal Press	2008
5	Introduction to Digital Video,	John Watkinson	Focal Press	2001

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://www.youtube.com/watch?v=M_nTmRtAD98
2	https://www.youtube.com/watch?v=aTDr79yvUus
3	https://www.youtube.com/watch?v=g_ysg46q-jQ
4	https://www.youtube.com/watch?v=4BaDaGTUgIY

SEMESTER S7

OPTIMIZATION TECHNIQUES

Course Code	**OEECT723**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Enable the learner to formulate engineering minima/maxima problems as optimization problems
2. Enable the learner to deploy various constrained and unconstrained optimization algorithms to obtain the minima/maxima of engineering problems

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Engineering application of Optimization – Statement of an Optimization problem–Classification, Review of basic calculus concepts –Stationary points; Functions of single and two variables; Convexity and concavity of functions –Definition of Global and Local optima – Optimality criteria, Linear programming methods for optimum design – Standard form of linear programming (LP) problem; Canonical form of LP problem; Simplex Method, Duality, Application of LPP models in engineering	**9**
2	Optimization algorithms for solving unconstrained nonlinear optimization problems – Search based techniques: Direct search: Fibonacci and golden section search , Hookes and Jeeves , Gradient based method: Newton's method	**9**
3	Optimization algorithms for solving constrained optimization problems– direct methods – penalty function methods, barrier method -Optimization of function of multiple variables subject to equality constraints; Lagrangian	**9**

	function– Inequality constrained techniques-KKT conditions-constrained steepest descent method	
4	Modern methods of Optimization– Metaheuristic techniques: Genetic Algorithms – Simulated Annealing – Particle Swarm optimization –Ant colony optimization– : Use of Matlab/Scilab to solve optimization problem	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Formulate an optimization problem to optimize an engineering application using the principles of basic calculus.	**K2**
CO2	Apply the Simplex method to solve a linear programming problem	**K3**
CO3	Solve the unconstrained optimization problems using gradient based method.	**K3**
CO4	Apply the various optimization techniques to solve a constrained optimization problem	**K3**
CO5	Use metaheuristic algorithms to solve constrained and unconstrained	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**	**2**									**2**
CO2	**3**	**3**	**3**									**2**
CO3	**3**	**2**	**3**									**2**
CO4	**3**	**2**	**3**									**2**
CO5	**3**	**2**	**3**									**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Engineering Optimization, Theory and Practice	S.S RAO	New Age International Publishers	4th Edition ,2012

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Optimization Techniques and Applications with Examples	Xin-She Yang	John Wiley & Sons	2018
2	Optimization for Engineering Design Algorithms and Examples	Deb K	Prentice Hall India	2000
3	Introduction to Optimization Design	Arora J	Elsevier Academic Press, New Delhi	2004
4	Linear Programming	Hardley G	Narosa Book Distributors Private Ltd	2002
5	Genetic Algorithms and engineering optimization	Mitsuo Gen, Runwei Cheng	John Wiley & Sons	2002
6	An introduction to optimization	Edwin KP Chong, Stanislaw, H Hak	John Wiley & Sons	Fourth Edition, 2013

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	NPTEL https://www.youtube.com/watch?v=a2QgdDk4Xjw
2	NPTEL https://www.youtube.com/watch?v=dPQKltPBLfc
3	NPTEL https://www.youtube.com/watch?v=qY-gKL7GxYk
4	NPTEL https://www.youtube.com/watch?v=Z_8MpZeMdD4 https://www.youtube.com/watch?v=FKBgCpJlX48

SEMESTER 8

Electronics Engineering (VLSI Design and Technology)

SEMESTER S8

MEMORY DESIGN AND IN-MEMORY COMPUTING

Course Code	PEEVT 861	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT503 VLSI Technology	Course Type	Elective

Course Objectives:

1. To provide an understanding of various memory types and their applications, emphasizing SRAM cell design, optimization, and the principles of memory operation in integrated circuits.

2. To enable students to design and evaluate DRAM and Flash memory systems, focusing on cell design, refresh mechanisms, memory array organization, and the intricacies of programming, erasing, and error correction.

3. To equip students with the skills to analyse timing and signal integrity in memory circuits, and to apply power optimization techniques, including power-gating and clock-gating, to enhance the efficiency of memory systems.

4. To explore in-memory computing techniques and emerging memory technologies, and to understand their applications in non-volatile storage, scientific computing, signal processing, and deep learning.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Memory Design: Overview of memory types and their applications, Importance of memory design in integrated circuits, Basic principles of memory operation. Static Random-Access Memory (SRAM): SRAM cell design and optimization, Memory bit-cell stability and read/write operations, SRAM array architecture and peripheral circuitry.	9

2	Dynamic Random-Access Memory (DRAM): DRAM cell design and refresh mechanisms, Memory array organization and addressing, Timing considerations in DRAM design. Flash Memory: NAND and NOR Flash architectures, Programming and erasing mechanisms, Wear levelling and error correction in Flash memory.	**9**
3	Timing and Signal Integrity: Setup and hold time analysis, Clock-to-q delay considerations, Signal integrity challenges in memory circuits. Power Optimization in Memory Systems: Active and standby power consumption in memory, Power-gating and clock gating techniques, Low-power design strategies for memory circuits. Emerging Memory Technologies: Overview of emerging memory technologies.	**9**
4	In-memory computing: Memory devices and applications, Memory devices and computational primitives, Charge-based memory devices & Computational primitives, Resistance-based memory devices & Computational primitives, Phase change memory. Applications: Non-volatile binary storage, Scientific computing, Signal processing & Optimization, Deep learning.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand and design various memory types, including SRAM, by applying fundamental principles of memory operation and optimizing SRAM cell stability and array architecture.	**K2**
CO2	Design and analyse DRAM and Flash memory systems, focusing on cell design, refresh mechanisms, array organization, and addressing, as well as programming, erasing, and error correction techniques.	**K4**
CO3	Perform timing and signal integrity analysis in memory circuits and apply power optimization techniques, including power-gating and clock-gating, to enhance the efficiency of memory systems.	**K3**
CO4	Explore and implement in-memory computing techniques and emerging memory technologies, understanding their applications in non-volatile storage, scientific computing, signal processing, and deep learning.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**	**1**	**1**	**1**	**2**	**1**						
CO2	**2**	**2**	**3**	**2**	**2**	**1**						
CO3	**2**	**1**	**2**	**1**	**2**	**1**						
CO4	**2**	**1**	**2**	**1**	**2**	**1**						

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Memory Chip Design	Kiyoo Itoh	Springer	2013
2	VLSI-Design of Non-Volatile Memories.	G Campardo, R. Micheloni, D. Novosel	Springer	2005
3	Extreme Statistics in Nanoscale Memory Design	Amith Singhee, Rob A Rutenbar	Springer	2010.

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Resistive Random Access Memory (RRAM): From Devices to Array Architectures	Shimeng Yu	Springer Nature	2022
2	High-Bandwidth Memory Interface	Chulwoo Kim, Hyun-Woo Lee, Junyoung Song	Springer	2013
3	Memory Systems: Cache, DRAM, Disk	Bruce Jacob, Spencer Ng, David Wang	Morgan Kaufmann	2010

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/101/117101058/
2	https://www.youtube.com/watch?v=OeRk8XZnk0s
3	https://onlinecourses.nptel.ac.in/noc24_ee67/preview
4	https://www.youtube.com/watch?v=BTnr8z-ePR4

SEMESTER S8

POWER SEMICONDUCTOR DEVICES

Course Code	**PEEVT 862**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT503 VLSI Technology	**Course Type**	Elective

Course Objectives:

1. To introduce the fundamental concepts and historical evolution of high-power circuit design, emphasizing power levels, efficiency, and thermal considerations in various industrial applications.
2. To provide an understanding of high-power design methodologies, focusing on techniques for optimizing efficiency and reliability in circuits, and in-depth knowledge of power semiconductor devices such as MOSFETs and IGBTs
3. To equip students with the principles and design considerations for high-frequency converters and power amplifiers, including effective thermal management strategies for high-power systems.
4. To explore real-world applications and case studies of high-power circuit designs, and to investigate advanced topics and emerging trends to enhance efficiency and reliability in high-power systems.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to High Power Circuit Design: Overview of the importance of high-power circuit design in various industries, Historical context and evolution of high-power technologies, Introduction to key concepts: power levels, efficiency, and thermal considerations.	**9**
2	Design Methodologies for High Power Applications: Principles of high-power design methodologies, Techniques for optimizing efficiency and reliability in high-power circuits. Power Semiconductor Devices and Applications: In-depth study of power semiconductor devices (MOSFETs, & IGBTs). Applications of power	**9**

	devices in high-power circuits.	
3	High-Frequency Converters and Power Amplifiers: Principles of high-frequency converters and power amplifiers, Design considerations and challenges in high-frequency power conversion. Thermal Management in High Power Systems: Principles of thermal management for high-power circuits, Heat dissipation strategies and thermal modelling.	**9**
4	Applications of High-Power Circuit Design: Real-world applications of high-power circuit designs. Case studies: Analysing successful high-power system implementations. Advanced Topics and Emerging Trends in High Power Design: Emerging trends in high-power circuit design, Advanced components and techniques for achieving higher efficiency and reliability.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
● 2 Questions from each module. ● Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	● Each question carries 9 marks. ● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the significance of high-power circuit design, including its historical evolution, key concepts such as power levels, efficiency, and thermal considerations relevant to various industries.	**K2**
CO2	Apply design methodologies for high-power applications, optimizing efficiency and reliability by understanding the principles and techniques associated with power semiconductor devices like MOSFETs and IGBTs.	**K3**
CO3	Design and analyse high-frequency converters and power amplifiers, addressing design considerations and challenges, and implement effective thermal management strategies for high-power systems.	**K4**
CO4	Evaluate real-world applications of high-power circuit design through case studies, and explore advanced topics and emerging trends to enhance efficiency and reliability in high-power circuit implementations	**K5**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**	**2**	**1**	**1**	**1**			**1**	**1**		
CO2	**3**	**2**	**3**	**2**	**1**	**1**			**1**	**1**		
CO3	**3**	**3**	**3**	**2**	**3**	**1**			**1**	**1**		
CO4	**3**	**3**	**3**	**3**	**1**	**1**			**1**	**1**		

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of High-Frequency CMOS Analog Integrated Circuits.	Duran Leblebici, Yusuf Leblebici	Cambridge	2009
2	High-Frequency Integrated Circuits	Sorin Voinigescu	Cambridge	2013
3	The Design of CMOS Radio-Frequency Integrated Circuits	Thomas H. Lee	Cambridge	2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Transmission Lines: Equivalent Circuits, Electromagnetic Theory, and Photons	Richard Collier	Cambridge University Press	2013
2	Dynamic Power Supply Transmitters: Envelope Tracking, Direct Polar, and Hybrid Combinations	Earl McCune	Cambridge University Press	2015
3	RF Circuit Design	Ludwig	Pearson	2011

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106089/
2	www.digimat.in/nptel/courses/video/108108112/
3	https://archive.nptel.ac.in/courses/108/102/108102157/
4	https://archive.nptel.ac.in/courses/117/106/117106089/

SEMESTER S8

MIXED SIGNAL CIRCUIT DESIGN

Course Code	**PEEVT 863**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Analog VLSI design (Course code)	**Course Type**	Theory

Course Objectives:

1. To give the knowledge about various analog and digital CMOS circuits
2. To impart the skill in analysis and design of analog and digital CMOS circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	CMOS Amplifiers- Common Source with diode connected loads and current source load, CS stage with source degeneration, CG stage and Source Follower (Only Voltage Gain and Output impedance of circuits) Differential Amplifiers-Differential Amplifier with MOS current source Load, with cascaded load and with current mirror load, MOS telescopic cascode amplifier. (Only Voltage Gain and Output impedance of circuits)	11
2	Band gap References- Supply Independent Biasing, Temperature independent references –band gap reference Phase Locked Loop – Simple PLL , Basic PLL Topology, Charge Pump PLL, Basic Charge Pump PLL	9
3	Dynamic analog circuits – charge injection and capacitive feed through in MOS switch, Reduction technique, Switched Capacitor Circuits- sample and hold circuits, Switched Capacitor Integrator, Ladder filters	11
4	DAC Specifications-DNL, INL, latency, SNR, Dynamic Range, DAC	9

	Architecture - Resistor String, Charge Scaling and Pipeline types. ADC Specifications-Quantization error, Aliasing, SNR, Aperture error, ADC Architecture- Flash and Pipe line types.	

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	To analyse the CMOS amplifiers and differential amplifiers	**K4**
CO2	To understand the band gap references and PLL Concepts	**K2**
CO3	To analyse the dynamic analog circuits and Switched capacitor circuits	**K4**
CO4	To understand the DAC and ADC circuits	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**2**									
CO2	**3**	**2**	**2**									
CO3	**3**	**3**										
CO4	**3**	**2**										**1**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design	Phillip E. Allen, Douglas R. Holbery	Oxford	2004.
2	Fundamentals of Microelectronics	Razavi B.	Wiley student Edition	2014.

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS: Circuits Design, Layout and Simulation	Baker, Li, Boyce	Prentice Hall India	2000
2	Design of Analog CMOS Integrated Circuits	Razavi B.	Mc Graw Hill	2001

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/101/117101105/
2	https://www.youtube.com/watch?v=7xVSL93ZZq8&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&inde
3	https://www.youtube.com/watch?v=z5yaC4oEHLk
4	https://www.youtube.com/watch?v=8LuofneTOF8

SEMESTER S8

DIGITAL IMAGE PROCESSING

Course Code	**PEEVT 864**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Signal Processing (Course code)	**Course Type**	Theory

Course Objectives:

1. To study the image fundamentals and transforms necessary for image processing.
2. To familiarize different image processing techniques

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Digital Image Fundamentals-Elements of visual perception, image sensing and acquisition, image sampling and quantization, basic relationships between pixels – neighborhood, adjacency, connectivity, distance measures. Brightness, contrast, hue, saturation, mach band effect, Colour image fundamentals-RGB, CMY, HIS models, 2D sampling, quantization.	**9**
2	Image Enhancement: Spatial domain methods: point processing-intensity transformations, histogram processing, image subtraction, image averaging, geometric transformation Sharpening filters – first and second derivative, two-dimensional DFT and its inverse, frequency domain filters – low-pass and high-pass.	**9**
3	Image segmentation: Classification of Image segmentation techniques, region approach, clustering techniques. Classification of edges, edge detection Image restoration: Restoration Models, Linear Filtering Techniques: Inverse and Wiener	**9**
4	Image Compression- Need for compression, redundancy, classification of image compression schemes,–inter-pixel and psycho-visual; Lossless compression – predictive, Lossy compression- predictive and transform coding –DCT, (basics only); Still image compression standards – JPEG .	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the various concepts and mathematical transforms for image transform	**K2**
CO2	Interpret the various image enhancement techniques	**K2**
CO3	Illustrate the image segmentation algorithm	**K2**
CO4	Summarise basic image compression techniques	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**1**										**2**
CO2	**3**	**2**			**2**							**2**
CO3	**3**	**2**			**2**							**2**
CO4	**3**	**2**			**2**							**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Image Processing	Gonzalez Rafel C	Pearson Education	2009
2	Digital Image Processing	S Jayaraman, S Esakkirajan, T Veerakumar	Tata Mc Graw Hill	2015

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of Digital Image Processing	Jain Anil K	PHI	1988
2	Digital image processing	Kenneth R Castleman	Pearson Education,	2/e,2003
3	Digital Image Processing	Pratt William K	John Wiley	4/e,2007

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117105135
2	https://nptel.ac.in/courses/117105135
3	https://nptel.ac.in/courses/117105135
4	https://nptel.ac.in/courses/117105135

SEMESTER S8

ROBOTICS

Course Code	PEEVT 866	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. Impart knowledge about the engineering aspects of Robots.
2. Discuss the various sensors and actuators used in robotic manipulator.
3. Practice forward and inverse kinematic calculations of known robotic manipulators.
4. Teach the method of Trajectory planning calculation.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction:** Definition and origin of robotics, Robot Anatomy, Robot specifications, **Robot characteristics:** accuracy, precision, and repeatability, Areas of application, classification of robots. **Robotic arm:** Components and structure, Types of joints and workspace, Common kinematic arrangements, Wrists, End effectors.	9
2	**Sensors:** Types and applications of sensors in Robotics, position and displacement sensors, Strain gauge based force torque sensors, Tachometers. **Robotic vision systems:** Imaging, Sensing and Digitization, Image processing techniques, Areas of application in robotics. **Robotic drive systems and actuators:** Hydraulic, Pneumatic and Electric drives. Specification, principle of operation and areas of application of: Stepper motor, Servo motor and brushless DC motor. Microprocessor control of electric motors, speed control using PWM and direction control	9

	using H- Bridge.	
3	**Introduction to kinematics:** Position and orientation of objects, Rotation, Euler angles, Rigid motion representation using Homogenous Transformation matrix. **Forward kinematics:** Link coordinates, Denavit-Hartenberg Representation, Application of DH convention to different serial kinematic arrangements fitted with spherical wrist. **Inverse kinematics**: General properties of solutions, Kinematic Decoupling, Inverse kinematic solutions for all basic types of three-link robotic arms fitted with a spherical wrist.	**9**
4	**Velocity kinematics:** Derivation of the Jacobian, Application of velocity kinematics for serial manipulators, importance of Singularities. **Manipulator Dynamics:** Introduction to Legrangian mechanics and Dynamic equation for 2 DOF robots, Introduction to position control and force control of robotic manipulators. **Trajectory Planning:** Joint space Vs Cartesian space, Joint space trajectory planning	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Identify the anatomy of robotic manipulators used in industry.	**Understand**
CO2	Identify the sensors and actuators required for robotic manipulators.	**Understand**
CO3	Determine the forward and inverse kinematics of robotic manipulators.	**Apply**
CO4	Determine the dynamics and path planning of robotic manipulators.	**Apply**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	2	-	-	-	-	-	-	-	-	2
CO2	2	3	2	-	-	-	-	-	-	-	-	2
CO3	2	3	2	-	-	-	-	-	-	-	-	2
CO4	2	3	2	-	-	-	-	-	-	-	-	2
CO5	2	3	2	-	-	-	-	-	-	-	-	2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introduction to Robotics. Analysis, control, applications	Saeed B. Niku	Wiley student edition	2nd Edition, 2010
2	Industrial Robotics – Technology, Programming and Applications	Mikell and Groover	McGraw Hill	2nd Edition, 2012

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Robotics: Fundamental concepts and analysis	Ashitava Ghosal	OXFORD University Press	2006 Edition
2	Robot Dynamics and Control	Spong and Vidyasagar	Wiley Student Edition	2008 Edition
3	Fundamentals of Robotics: Analysis & Control	Robert J. Schilling	Pearson Education	2000 Edition

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/j8vYClEnyk0 https://youtu.be/o0NLi-wJS1I https://youtu.be/MH26PuRNMXM https://youtu.be/Ra-R0ZCdkPc https://youtu.be/8lCTkf-qjA0 https://youtu.be/KMqWSypAuEg https://youtu.be/nLRoK6Hyj0w https://youtu.be/uMxmBVX1pAQ https://youtu.be/xKzAqwpT06A
2	https://youtu.be/sCTgZv33tuA https://youtu.be/T6kGQrnUYD8 https://youtu.be/NcK9vlcdvZs https://youtu.be/rYaTu3Y2DMY https://youtu.be/HITCMaNCFQ8 https://youtu.be/HQgU76ZOP0o
3	https://youtu.be/wcy0Y3Jgf14 https://youtu.be/9Xyy24mbLQ0 https://youtu.be/kw64yS6vH14 https://youtu.be/6Wb0rmIvIlI https://youtu.be/AbRhzpReb2Q https://youtu.be/h4_2xAPj3y0 https://youtu.be/Zh55IM043rY https://youtu.be/iENLo_dxCZI https://youtu.be/NibHkkg2CQU https://youtu.be/93xncDTKqT4
4	https://youtu.be/B67ug1yx13E https://youtu.be/mXxEp5Q6dA8 https://youtu.be/thGicrIgtv0 https://youtu.be/irfHrA4fSDw https://youtu.be/O6ZbUDSFg_o https://youtu.be/kpiF_f_AntI https://youtu.be/zSvCAW-mowg https://youtu.be/OVGH_e0kjSE

SEMESTER S8
CLOUD COMPUTING

Course Code	**PEEVT 867**	**CIE Marks**	60
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	40
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Understand Cloud Computing Fundamentals.
2. Explore Cloud Technologies and Platforms.
3. Apply Cloud Solutions and Ensure Security.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Traditional computing- Limitations. Overview of Computing Paradigms- Grid Computing, Cluster Computing, Distributed Computing, Utility Computing, Cloud Computing. NIST reference Model-Basic terminology and concepts. Cloud characteristics, benefits and challenges, Roles and Boundaries. Cloud delivery (service) models-Infrastructure-as-a-Service (IaaS), Platform-as-a-Service (PaaS), Software-as-a-Service (SaaS), XaaS (Anything-as-a-service) - Cloud deployment models- Public cloud, Community cloud, Private cloud, Hybrid cloud.	**8**
2	Introduction to virtualization-Virtualizing physical computing resources, Virtual Machines (Machine virtualization), non-virtualized v/s virtualized machine environments. Types of VMs- process VM v/s system VM, Emulation, interpretation and binary translation. Hardware-level virtualization- Hypervisors/VMM. Types of Hypervisors. Full Virtualization, Para- Virtualization, Hardware-assisted virtualization, OS level virtualization. Basics of Network Virtualization, Storage Virtualization and Desktop Virtualization, Pros and cons of virtualization.	**8**

3	Broadband networks and internet architecture- Internet Service Providers (ISPs), Data center technology, Web technology, Multitenant technology, Service technology. Resource provisioning techniques-static and dynamic provisioning. Open-source software platforms for private cloud-OpenStack, Cloud Stack, Basics of Eucalyptus, Open Nebula, Nimbus. Cloud Programming- Parallel Computing and Programming Paradigms. Map Reduce – Hadoop Library from Apache, HDFS, Pig Latin High Level Languages, Apache Spark.	**8**
4	Basic terms and concepts in security- Threat agents, Cloud security threats/risks, Trust. Operating system security-Virtual machine security-Security of virtualization- Security Risks Posed by Shared Images, Security Risks Posed by Management OS. Infrastructure security- Network Level Security, Host Level Security, Application level security, Security of the Physical Systems. Identity & Access Management- Access Control. **Amazon Web Services (AWS)**:- AWS ecosystem- Computing services, Amazon machine images, Elastic Compute Cloud (EC2), Advanced compute services. Storage services-Simple Storage System (Amazon S3), Elastic Block Store (Amazon EBS). **Google Cloud Platform**:- IaaS Offerings: Compute Engine (GCE), Cloud Storage, PaaS Offerings: Google App Engine (GAE), Storage services, Application services, Compute services, Database Services, SaaS Offerings: Gmail, Docs, Google Drive. **Microsoft Azure:** Azure Platform Architecture, Hyper-V, Azure Virtual Machine, Compute services, Storage services.	**12**

Course Assessment Method
(CIE: 60 marks, ESE: 40 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**30**	**12.5**	**12.5**	**60**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 2 marks **(8x2 =16 marks)**	• Each question carries 6 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x6 = 24 marks)**	**40**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain the various cloud computing models and services.	K2
CO2	Demonstrate the significance of implementing virtualization techniques.	K2
CO3	Explain different cloud enabling technologies and compare private cloud platforms	K2
CO4	Apply appropriate cloud programming methods to solve big data problems	K3
CO5	Describe the need for security mechanisms in cloud and compare the different popular cloud computing platforms	K2

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**											**3**
CO2	**2**	**2**	**3**									**3**
CO3	**3**											**3**
CO4	**2**	**2**	**3**	**3**	**2**							**3**
CO5	**3**	**3**			**3**							**3**

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Cloud Computing Concepts, Technology &Architecture	Thomas, E., Zaigham M., Ricardo P	Prentice Hall	2013
2	Mastering cloud computing: foundations and applications programming	Buyya, R., Vecchiola, C., & Selvi, S. T.	Morgan Kaufmann	2017
3	Cloud computing	Bhowmik, S	Cambridge University Press	2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Cloud computing: theory and practice	Marinescu, D. C	Morgan Kaufmann	2017
2	Cloud computing: Principles and paradigms	Buyya, R., Broberg, J., & Goscinski, A. M	John Wiley & Sons.	2011

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/106/105/106105167/
2	https://onlinecourses.nptel.ac.in/noc23_cs90/preview
3	https://onlinecourses.nptel.ac.in/noc22_cs18/preview
4	https://archive.nptel.ac.in/courses/106/105/106105167/

SEMESTER S8

MIXED-SIGNAL VLSI DESIGN

Course Code	**PEEVT 865**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	5/3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT601 Analog VLSI Design, PCEVT50 Digital CMOS Design	**Course Type**	5 Credit Elective

Course Objectives:

1. To provide students with a comprehensive understanding of CMOS amplifier design, including small-signal modelling, frequency response analysis, and the implementation of various amplifier configurations such as common source, cascode, and folded cascode amplifiers.
2. To equip students with the skills to design and analyze CMOS differential amplifiers, including the use of current mirrors and techniques to enhance common-mode rejection ratio (CMRR), and to understand their application in high-performance circuits.
3. To familiarize students with the design and optimization of two-stage operational amplifiers, focusing on frequency compensation techniques like Miller compensation, and the development of stable bandgap references for reliable operation.
4. To teach the principles of data converter design, including DAC and ADC architectures, and to enable them to understand and implement various data conversion techniques such as resistor string, R-2R ladder, and different ADC types.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**CMOS Amplifiers** **MOS small signal model:** **CMOS Amplifiers**: Common source amplifier with resistive and active loads, Common source amplifier with source degeneration, Common gate and Common drain amplifier (only voltage gain and input and output	**9**

	impedances of the circuits), Frequency Response of CMOS Amplifiers **Cascode Amplifier:** Cascoded amplifier with cascade loads Folded cascode Amplifier.	
2	**CMOS Differential Amplifiers** **MOS Current Mirror:** Basic circuit, PMOS and NMOS current mirrors Simple and Cascode current mirror circuits. **CMOS Differential Amplifier:** Differential Amplifier with resistive, current source and current mirror loads, MOS telescopic cascode amplifier (only voltage gain and input and output impedance of the circuits) **Common-Mode Rejection Ratio (CMRR) and its Enhancement:** methods to measure and improve CMRR, and techniques such as common-mode feedback to enhance performance in noisy environments	**9**
3	**CMOS Operational Amplifier** **Two Stage Operational Amplifiers** Frequency compensation of OPAMPS Miller compensation**.** **Band gap References-** Supply Independent Biasing, Temperature independent references –band gap reference	**9**
4	**Data Converters:** DAC specifications, ADC specifications **DAC Architecture -** Resistor String, R-2R Ladder Networks, Current Steering, Charge Scaling, cyclic and Pipeline types. **ADC Architecture-** Flash type, The Successive approximation type and oversampling ADCs.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

Criteria for Evaluation (Evaluate and Analyse): 20 marks

1. Literature Review and Report (10 Marks)

Assessment Method:

- Students select recent publications on a specific topic related to the course (eg. Differential Amplifier Design).
- Preparation of a report summarizing the findings, discussing the significance, and proposing future research directions.

Criteria:

- Relevance of Chosen Publications (2 Marks): Selection of up-to-date and significant research papers.
- Depth of Analysis (4 Marks): Thorough understanding and critical analysis of the literature.
- Clarity and Organization (2 Marks): Well-structured report with clear arguments.
- Originality (2 Marks): Innovative insights or perspectives.

3. Design Exercise (10 Marks)

Design a CMOS differential amplifier meeting specific requirements such as gain, input impedance, and common-mode rejection ratio (CMRR). Present the design through a schematic diagram and perform calculations to verify that the design meets the given specifications.

Criteria for Assessment:

1. **Design Accuracy (4 marks)**
    - Correct implementation of the differential amplifier design.
    - Accuracy in meeting the specified design parameters, such as gain, impedance, and CMRR.
2. **Calculation and Analysis (3 marks)**
    - Correctness and thoroughness of calculations related to amplifier performance.

- Proper analysis and justification of design choices.

3. **Schematic Presentation (2 marks)**
   - Clarity and correctness of the schematic diagram.
   - Proper labelling and organization of the components in the schematic.
4. **Design Justification (1 mark)**
   - Clear explanation of design choices and how they address the problem requirements.
   - Insight into the trade-offs made during the design process.

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Design and analyse various CMOS amplifiers, including common source, common gate, and common drain amplifiers, as well as cascode and folded cascode amplifiers, with an understanding of their frequency response and small-signal models.	**K3**
CO2	Implement and evaluate CMOS differential amplifiers with various loads, apply MOS current mirrors, and enhance common-mode rejection ratio (CMRR) using techniques such as common-mode feedback in noisy environments.	**K3**
CO3	Design and optimize two-stage operational amplifiers, apply frequency compensation techniques including Miller compensation, and develop bandgap references for stable supply-independent and temperature-independent biasing.	**K3**
CO4	Analyse and design data converters, including DACs and ADCs, by understanding their specifications, architectures, and various types such as resistor string, R-2R ladder, current steering, flash, successive approximation, and oversampling ADCs.	**K4**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**	**3**	**2**	**2**	**3**	**1**	**1**		**1**			
CO2	**2**	**3**	**2**	**2**	**3**	**1**	**1**		**1**			
CO3	**2**	**3**	**2**	**2**	**3**	**1**	**1**		**1**			
CO4	**2**	**3**	**2**	**3**	**2**	**1**	**1**		**1**			

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design of Analog CMOS Integrated Circuits	Behzad Razavi	McGraw-Hill	2/e, 2002
2	CMOS: Circuits Design, Layout and Simulation,	Baker, Li, Boyce,	Prentice Hall India,	2000
3	Microelectronic Circuits	Sedra & Smith	Oxford University Press	6/e,2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design,	Phillip E. Allen, Douglas R. Holbery	Oxford University Press	3/e
2	Fundamentals of Microelectronics	Behzad Razavi	Wiley student Edition	2014
3	Analysis and Design of Analog Integrated Circuits	Meyer Gray , Hurst, Lewis	Wiley	5/e, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc22_ee37/preview
2	https://archive.nptel.ac.in/courses/117/101/117101106/
3	https://onlinecourses.nptel.ac.in/noc22_ee27/preview
4	https://nptel.ac.in/courses/117106034

SEMESTER S8

PATTERN RECOGNITION

Course Code	OEEVT 831	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304	Course Type	Theory

Course Objectives:

1. To introduce the fundamental algorithms for pattern recognition
2. To instigate the various classification and clustering techniques

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction: Basics of pattern recognition system, various applications, Machine Perception, classification of pattern recognition systems Design of Pattern recognition system, Pattern recognition Life Cycle. Statistical Pattern Recognition: Review of probability theory, Gaussian distribution, Bayes decision theory and Classifiers	8
2	Concept of feature extraction and dimensionality, Curse of dimensionality, Hidden Markov Models (HMM) - basic concepts, Gaussian mixture models. Non-Parametric methods: Non-parametric techniques for density estimation - Parzen-window method, K-Nearest Neighbour method.	9
3	Decision trees: Construction, splitting of nodes, choosing of attributes, overfitting, pruning Linear Discriminant based algorithm: Perceptron, Support Vector Machines	9
4	Multilayer perceptrons, Back Propagation Algorithms. Artificial Neural Networks Classifier Ensembles: Bagging, Boosting/ AdaBoost Unsupervised learning: Clustering - Criterion functions for clustering, Algorithms for clustering: K-means and Hierarchical methods, Cluster validation	10

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	60

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design a pattern recognition system	K2
CO2	Know the major approaches in statistical and syntactic pattern recognition.	K2
CO3	Become aware of the theoretical issues involved in pattern recognition system design such as the curse of dimensionality.	K2
CO4	Implement pattern recognition technique	K3

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2										3
CO2	2	2										3
CO3	2	2										3
CO4	2	2										3

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Pattern Recognition and Machine Learning,	C M Bishop	Springer	2006
2	Pattern Classification and scene analysis,	R O Duda, P.E. Hart and D.G. Stork,	John Wiley	2nd edition, 2001

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Pattern Recognition Engineering	Morton Nadler, Eric P. Smith	John Wiley & Sons, New York	1993.
2	Pattern Recognition : Statistical, Structural and Neural Approaches	Robert J. Schalkoff	John Wiley & Sons Inc. New York	2007
3	Pattern Recognition	S.Theodoridis and K. Koutroumbas	Academic Press	4/e,2009
4	Machine Learning	Tom Mitchell	McGraw Hill	1997
5	Pattern Recognition Principles	Tou, J.T. and Gonzalez, R.C.	Addison-Wesley Publishing Company,	1974

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://www.youtube.com/watch?v=mfePdDh9t6Q
2	https://www.youtube.com/watch?v=yG1nETGyW2E
3	https://www.youtube.com/watch?v=pMHOPezBUfU
4	https://youtu.be/EWmCkVfPnJ8?si=re_1ZpaXCtOohvwq

SEMESTER S8

MACHINE LEARNING

Course Code	OEEVT 832	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To understand basics of machine learning and different types
2. To understand different machine learning algorithms.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Basics of machine learning, supervised and unsupervised learning, examples, features, feature vector, training set, target vector, test set, feature extraction, over-fitting, curse of dimensionality. Review of probability theory, Gaussian distribution, decision theory.	9
2	Regression: linear regression, error functions in regression, multivariate regression, regression applications, bias and variance. Classification : Bayes' decision theory, discriminant functions and decision surfaces, Bayesian classification for normal distributions, classification applications.	9
3	Linear discriminant based algorithm: perceptron, gradient descent method, perceptron algorithm, support vector machines, separable classes, non-separable classes, multiclass case.	9
4	Unsupervised learning: Clustering, examples, criterion functions for clustering, proximity measures, algorithms for clustering. Ensemble methods: boosting, bagging. Basics of decision trees, random forest, examples. Dimensionality reduction: principal component analysis, Fischer's discriminant analysis. Evaluation and model Selection: ROC curves, evaluation measures, Confusion matrix, recall, precision, accuracy.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Describe basics of machine learning and types.	**K2**
CO2	Differentiate regression and classification, apply Bayes' decision theory in classification	**K3**
CO3	Apply linear algebra and statistical methods in discriminant based algorithms	**K3**
CO4	Illustrate the basics of unsupervised learning, non-metric methods, ensemble methods, dimensionality reduction, evaluation, model selection.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	-	-	-	-	-	-	-	-
CO2	3	2	2		2	-	-	-	-	-	-	-
CO3	3	2	2		2	-	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Pattern Recognition and Machine Learning	Bishop, C. M.	Springer, New York	2006
2	Pattern Recognition	Theodoridis, S. and Koutroumbas, K.	Academic Press, San Diego	2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	The Elements of Statistical Learning	Hastie, T., Tibshirani, R. and Friedman, J.	Springer	2001
2	Pattern Classification	Duda, R.O., Hart, P.E.	Wiley, New York	2001

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc23_cs18/preview - Introduction to Machine Learning By Prof. Balaraman Ravindran, IIT Madras
2	https://onlinecourses.nptel.ac.in/noc23_cs18/preview - Introduction to Machine Learning By Prof. Balaraman Ravindran, IIT Madras
3	https://onlinecourses.nptel.ac.in/noc23_cs18/preview - Introduction to Machine Learning By Prof. Balaraman Ravindran, IIT Madras
4	https://onlinecourses.nptel.ac.in/noc23_cs18/preview - Introduction to Machine Learning By Prof. Balaraman Ravindran, IIT Madras

SEMESTER S8

COMPUTER VISION

Course Code	**OEEVT833**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. To develop the knowledge of various methods, algorithms and applications of Computer Vision.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Review of image processing techniques: Digital filters, linear filters- Homomorphic filtering, Point operators- Histogram, neighbourhood operators, thresholding Mathematical morphology, Binary shape analysis, Binary shape analysis, Erosion, Dilation, Opening and Closing, Hit-or-Miss Transform ,connectedness, object labelling and counting, Boundary descriptors – Chain codes. Properties of Binary Regions, Geometric Features, Statistical Shape Properties	9
2	Feature Detection and Image Synthesis,Edge detection – edges, lines, active contours, Split and merge, Mean shift and mode finding, Normalized cuts, Graph cuts, energy- based methods- Cranny's Algorithm, Corner detection, Harris corner detection algorithm. Hough transform-Line and curve detection.	9
3	Shape from X - Shape from shading, Photometric stereo, Texture Occluding contour detection. Motion Analysis- Regularization theory,Optical Flow: brightness constancy equation, aperture problem, Horn-Shunck method,	9

	Lucas-Kanade method. Structure from motion	
4	Object recognition-Shape correspondence and shape matching PCA,SVM, LDA, Bayes rule andML methods. Eigen faces,Face detection, Face recognition, Application: Scene analysis Examples of real time applications: In-vehicle vision system.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand digital filtering operations for CV applications.	**K2**
CO2	Apply basic morphological and boundary operators for Computer vision applications	**K3**
CO3	Apply edge, corner detection algorithms to locate objects in an image.	**K3**
CO4	Apply optical flow algorithms to detect moving objects in a video.	**K3**
CO5	Analyse a given scene using appropriate computer vision algorithms to detect/recognize objects and to implement it in real time practical applications.	**K4**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**2**		**2**						**2**	**3**
CO2	**3**	**3**	**2**		**2**						**2**	**3**
CO3	**3**	**3**	**3**		**2**						**2**	**3**
CO4	**3**	**3**	**3**		**2**						**2**	**3**
CO5	**3**	**3**	**3**		**2**						**2**	**3**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Computer and Machine Vision -Theory Algorithm and Practicalities	E. R .Davies	Academic Press,	2012.
2	Computer Vision: Algorithms and Applications	Richard Szeliski	ISBN 978-1- 84882-935-0, Springer	2011
3	Computer Vision: A Modern Approach	David Forsyth and Jean Ponce	Pearson India	2002

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Deep Learning,	Goodfellow, Bengio, and Courville,	MIT Press,.	2006
2	Mastering OpenCV with Practical Computer Vision Projects	Daniel Lelis Baggio, et al	Packt Publishing Limited,	2012
3	Computer Vision: Models, Learning, and Inference,	Simon J D Prince	Cambridge University Press	2012
4	Digital Image Processing and Computer Vision,	R. J. Schalkoff	John Wiley,	2004
5	Programming Computer Vision with Python: Tools and algorithms for analyzing images	Jan Erik Solem,	O'Reilly Media,	2012

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc19_cs58/preview
2	https://onlinecourses.nptel.ac.in/noc21_cs93/preview
3	https://onlinecourses.nptel.ac.in/noc24_ee38/preview

SEMESTER S8

SECURE COMMUNICATION

Course Code	OEEVT 834	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To understand network security services and mechanisms and the types of attacks

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	OSI security architecture, Security attacks – Passive attacks, Active attacks, Security services- Authentication, Access Control, Data Confidentiality, Data integrity, Nonrepudiation, Availability service. Model for network security. Symmetric cipher model, Cryptography, Crypto analysis, Substitution techniques- Hill Cipher, One time pad, Transposition Techniques	9
2	Finite Fields Groups, Rings and Fields, Modular arithmetic, Euclidian algorithm, Finite Fields of the form GF(p), Polynomial arithmetic	8
3	Block Cipher Principles – Stream Ciphers and Block Ciphers, Feistel Cipher, Feistel Decryption algorithm, The Data encryption standard, DES Decryption - Avalanche effect, The AES Cipher, substitute bytes transformation, Shift row transformation, Mix Column transformation	9
4	Public Key Cryptography, RSA and Key Management Principles of public key cryptosystems-Public key cryptosystems, Application for Public key cryptosystem requirements, Fermat's theorem, Euler's Totient Function, Euler's theorem, RSA algorithm, Key management, Distribution of public keys, Publicly available directory, Public key authority, public key certificates, Distribution of secret keys using public key cryptography, Public Key Encryption, Message Authentication Code, Hash function	10

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Illustrate network security services, mechanisms and the types of attacks and also to understand symmetric encryption process and different encryption techniques	**K2**
CO2	Apply the concepts of group, ring, field, modular arithmetic, Euclidean algorithm, Finite fields and polynomial arithmetic	**K3**
CO3	Outline the principles of modern symmetric ciphers like the Data Encryption Standard and Advanced Encryption Standard	**K2**
CO4	Describe the concepts of public key cryptography, RSA algorithm, key distribution and management for public key systems	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**										**2**
CO2	**3**	**3**										**2**
CO3	**3**	**2**										**2**
CO4	**3**	**2**										**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Cryptography and Network security: principles and practice	William Stallings	Prentice Hall of India	4th Edition, 2006

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Cryptography and Network security Tata McGraw-Hill,	Behrouz A. Forouzan	Tata McGraw-Hill	2008
2	Abstract Algebra	David S. Dummit& Richard M Foote	Wiley India Pvt. Ltd.	2nd Edition, 2008
3	Cryptography, Theory and Practice	Douglas A. Stinson	Chapman & Hall, CRC PressCompany, Washington	2005
4	Elliptic Curves: Theory and Cryptography	Lawrence C. Washington	Chapman & Hall, CRCPress Company, Washington	2008

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/106/105/106105162/ CRYPTOGRAPHY AND NETWORK SECURITY, PROF. SOURAV MUKHOPADHYAY Department of Computer Science and Engineering IIT Kharagpur
2	https://archive.nptel.ac.in/courses/106/105/106105162/ CRYPTOGRAPHY AND NETWORK SECURITY, PROF. SOURAV MUKHOPADHYAY Department of Computer Science and Engineering IIT Kharagpur
3	https://archive.nptel.ac.in/courses/106/105/106105162/ CRYPTOGRAPHY AND NETWORK SECURITY, PROF. SOURAV MUKHOPADHYAY Department of Computer Science and Engineering IIT Kharagpur
4	https://archive.nptel.ac.in/courses/106/105/106105162/ CRYPTOGRAPHY AND NETWORK SECURITY, PROF. SOURAV MUKHOPADHYAY Department of Computer Science and Engineering IIT Kharagpur